HARRIS SEMICONDUCTOR

Dear Intelligent Power Data Book User,

We are happy to provide you with the latest information from Harris Intelligent Power. Inside you will find four new data sheets, a new application note and new packaging section. This information supersedes the pages of the Intelligent Power Data Book (DB304) as shown in the Table of Contents of this Addendum. We will continue to provide you with the latest information as it becomes available.

Sincerely,

Alan Moore
Product Marketing Manager
Intelligent Power Products

IS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FL 32902-0883 407-724-7000 FAX 407-729-5691 TWX 510-959-6259

INTELLIGENT POWER
INTEGRATED CIRCUITS

DB304 ADDENDUM

HARRIS SEMICONDUCTOR

HIP5061

PRELIMINARY

October 1992

6A, High Efficiency Current Mode Controlled PWM Regulator

Features

- Single Chip Current Mode Control IC
- 60V, 5A On-Chip DMOS Transistor
- Thermal Protection
- Over-Current Protection
- 250kHz Operation
- On-Chip Reference Voltage - 5.1V
- Slope Compensation
- V_{DD} Clamp

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Description

The HIP5061 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. The standard "Boost", "Buck-Boost", "Cuk", "Forward", "Flyback" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies may be implemented with this single control IC.

Over-temperature and rapid short-circuit recovery circuitry is incorporated within the IC. These circuits can disable the drive to the power transistor to protect both the transistor and insure rapid restarting of the supply after the short circuit is removed.

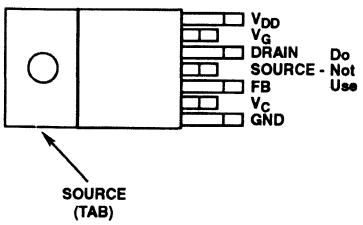
As a result of the power DMOS transistor's current and voltage capability (5A and 60V), power supplies with output power capability up to 50W are possible.

Ordering Information

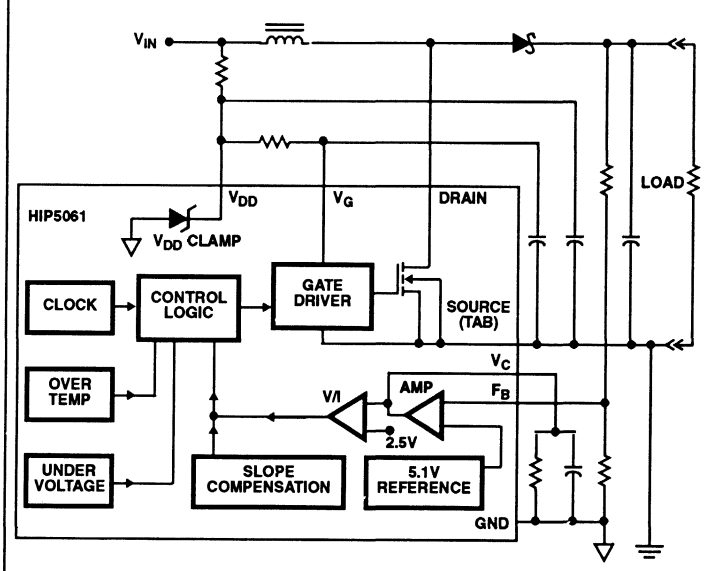
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5061DS	0°C to +85°C	7 Lead Staggered "Gullwing"

Pinout

7 LEAD STAGGERED "GULLWING"
TOP VIEW



Block Diagram



File Number **3390**

Absolute Maximum Ratings

DC Supply Voltage, V_{DD} ..... -0.3V to 16V
DC Supply Current, I_{DD} 105mA
DMOS Drain Voltage ..... -0.3V to 60V
Average DMOS Drain Current 5A
DMOS Source Voltage, V_{SOURCE}, TAB ..... -0.1V to 0.1V
DC Supply Voltage, V_G ..... -0.3V to V_{DD} + 0.3V
Compensation Pin Current, I_{VC} ..... -5mA to 35mA
Voltage at all Other Pins ..... -0.3V to V_{DD} + 0.3V
Operating Junction Temperature Range ..... 0°C to +105° C
Storage Temperature Range ..... -55° C to +150° C

Reliability Information

Thermal Resistance Junction-to-Case, θ_{JC} ..... 2°C/W
Maximum Package Power Dissipation at +85°C
(Depends Upon Mounting, Heat Sink and Application) 10W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = V_G =12V, V_C = 5V, V_{FB} = 5.1V, DRAIN = 0V, T_J = 0°C to 105°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DEVICE PARAMETERS						
I_{DD}	Quiescent Supply Current	V_{DD} = V_G = 13.2V, V_C = 0V	6	12	18	mA
I_{DD}	Operating Supply Current	V_{DD} = V_G = 13.2V, V_C = 8.5V, V_{FB} = 4V	-	20	31	mA
IV_G	Quiescent Current to Gate Driver	V_{DD} = V_G = 13.2V, V_C = 0V	-	0	10	µA
IV_G	Operating Current to Gate Driver	V_C = 3V	-	1	2	mA
V_{DDC}	Clamp Voltage	I_{DD} = 100mA	13.3	14	15	V
V_{REF}	Reference Voltage	I_{VC} = 0µA, V_C = V_{FB}	5.0	5.1	5.2	V
AMPLIFIERS						
I_{FB}	Input Current	V_{FB} = V_{REF}	-	-	0.5	µA
g_m (V_{FB})	V_{FB} Transconductance $I_{VC}/(V_{FB} - V_{REF})$	$/I_{VC}$ / = 500µA, Note 1	20	30	43	mS
IV_{CMAX}	Maximum Source Current	V_{FB} = 4.6V	-3.5	-2	-1	mA
IV_{CMAX}	Maximum Sink Current	V_{FB} = 5.6V	1	2	3.5	mA
A_{OL}	Voltage Gain	$/I_{VC}$ / = 500µA, Note 1	44	50	-	dB
V_{CMAX}	Short-Circuit Recovery Comparator Rising Threshold Voltage		5.5	7.0	8.9	V
V_{CHYS}	Short-Circuit Recovery Comparator Hysteresis Voltage		0.7	1.2	1.8	V
I_{VCOVER}	V_C Over-Voltage-Current	V_C = V_{CMAX}, V_{DD} = V_G = 10.8V	0	10	25	mA
CLOCK						
fq	Internal Clock Frequency		220	250	280	kHz
DMOS TRANSISTOR						
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, V_{DD} = V_G = 10.8V T_J = 25°C	-	0.15	0.22	Ω
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, V_{DD} = V_G = 10.8V T_J = 105°C	-	-	0.33	Ω
I_{DSS}	Drain-Source Leakage Current	V_{DRAIN} = 60V	-	1	10	µA

Electrical Specifications $V_{DD} = V_G = 12V$, $V_C = 5V$, $V_{FB} = 5.1V$, DRAIN = 0V, $T_J = 0°C$ to $105°C$, Unless Otherwise Specified (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DMOS TRANSISTOR (Continued)						
I_{DSH}	Average Drain Short Circuit Current	$V_{DRAIN} = 5V$, Note 2			5	A
C_{DRAIN}	DRAIN Capacitance	Note 2	-	200	-	pF
CURRENT CONTROLLED PWM						
$g_m(V_C)$	$\Delta I_{DRAIN,PEAK} / \Delta V_C$	Note 1	1.4	2.2	3.0	A/V
V/I_{REF}	Voltage to Current Converter Reference Voltage	$I_{DRAIN} = 0.25A$, Note 1	2.4	2.6	3.1	V
t_{BT}	Current Comparator Blanking Time	Note 1	40	100	175	ns
t_{ONMIN}	Minimum DMOS "ON" Time	Note 1	60	150	250	ns
t_{OFFMIN}	Minimum DMOS "OFF" Time	Note 1	40	100	200	ns
MINCI	Minimum Controllable DMOS Peak Current	Note 1	--	100	250	mA
MAXCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 6% to 30%, Note 1	7	9.5	12	A
MAXCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 30% to 96%, Note 1	5	8	12	A
CURRENT COMPENSATION RAMP						
$\Delta I/\Delta t$	Compensation Ramp Rate	$\Delta I_{DRAIN,PEAK} / \Delta$Time, Note 1	-1.4	-0.8	-0.3	A/µs
t_{RD}	Compensation Ramp Delay	Note 1	1.3	1.5	1.8	µs
START-UP						
V_{DDMIN}	Rising V_{DD} Threshold Voltage	$V_{FB} = 4V$	9.3	10.3	10.8	V
V_{DDHYS}	Power-On Hysteresis	$V_{FB} = 4V$	0.3	0.45	0.6	V
V_{CEN}	Enable Comparator Threshold Voltage		1.0	1.5	2.0	V
R_{VC}	Power-Up Resistance	$4V < V_{DD} < 10.8V$, $V_C = 0.8V$	50	500	2300	Ω
THERMAL MONITOR						
T_J	Substrate Temperature for Thermal Monitor to Trip	Note 2	105	--	145	°C
T_{JHY}	Temperature Hysteresis	Note 2	--	5	--	°C

NOTES:

1. Test is performed on the wafer at +25°C only.
2. Determined by design, not a measured parameter.

HARRIS SEMICONDUCTOR

HV-2405E

UL RECOGNIZED

October 1992

World-Wide
Single Chip Power Supply

Features

- Direct AC to DC Conversion
- Wide Input Voltage Range.....15Vrms-275Vrms
- Dual Output Voltages Available
- Output Current..... up to 50mA
- Output Voltage.....5V to 24V
- Line and Load Regulation..... <2%
- UL Recognition, File # E130808

Applications

- Power Supply for Non-Isolated Applications
- Power Supply for relay control
- Dual Output Supply for OFF-LINE Motor Controls
- Housekeeping Supply for Switch-Mode Power Supplies

Ordering Information

PART NUMBER	OPERATING TEMPERATURE RANGE	PACKAGE DESCRIPTION
HV3-2405E-5	0°C to +75°C	8 Lead Plastic DIP
HV3-2405E-9	-40°C to +85°C	8 Lead Plastic DIP

Description

The HV-2405E is a single chip off line power supply that converts world wide AC line voltages to a regulated DC voltage. The output voltage is adjustable from $5V_{DC}$ to $24V_{DC}$ with an output current of up to 50mA. The HV-2405E can operate from input voltages between 15Vrms and 275Vrms as well as input frequencies between 47Hz to 200Hz (see Table 1 in section titled "Minimum Input Voltage vs Output Current" for details).

The wide input voltage range makes the HV-2405E an excellent choice for use in equipment which is required to operate from either 240V or 120V. Unlike competitive AC-DC convertors, the HV-2405E can use the same external components for operation from either voltage. This flexibility in input voltage, as well as frequency, enables a single design for a world wide supply.

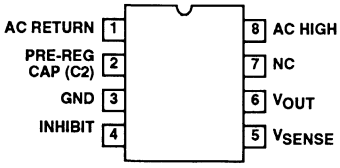
The HV-2405E has a safety feature that monitors the incoming AC line for large dv/dt (i.e. random noise spikes on AC line, initial power applied at or near peak line voltage). This inhibit function protects the HV-2405E, and subsequent circuitry, by turning off the HV-2405E during large dv/dt transients.This feature is utilized to ensure operation within the SOA (Safe Operating Area) of the HV-2405E.

The HV-2405E can be configured to work directly from an electrical outlet (see Figure 1) or imbedded in a larger system (see Figure 7). Both application circuits have components that will vary based on input voltage, output current and output voltage. It is important to understand these values prior to beginning your design.

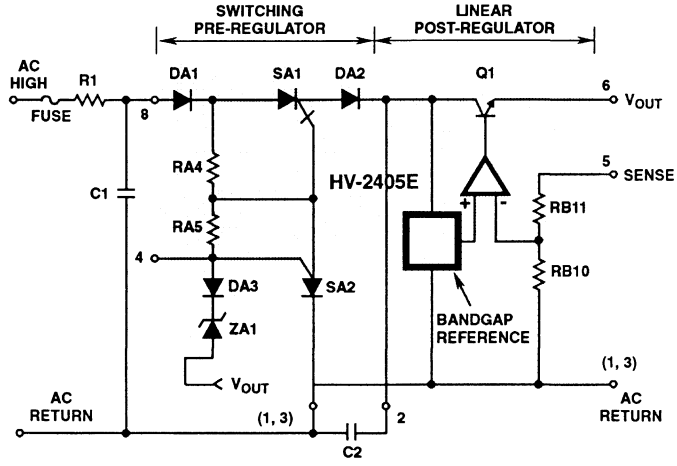
CAUTION: This Product Does Not Provide Isolation From The AC line. See Page 10 For General Precautions. Failure to use a properly rated fuse may cause R1 to reach dangerously High Temperature or Cause the HV-2405E to Crack or Explode.

Pinout

HV3-2405E (PLASTIC DIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2487.4**

Specifications HV-2405E

Absolute Maximum Ratings

Voltage Between Pin 1 and 8, Peak ..... ±500V
Voltage Between Pin 2 and 6 ..... 15V
Input Current, Peak 2A
Output Current 100mA
Output Voltage 34V

Operating Temperature Range

Maximum Junction Temperature ..... +150°C
HV3-2405E-9 ..... -40°C to +85°C
HV3-2405E-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Plastic DIP	91.8	29.6

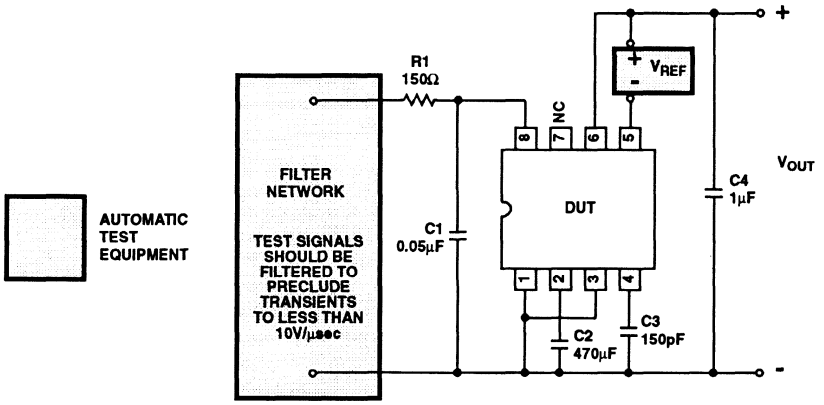
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

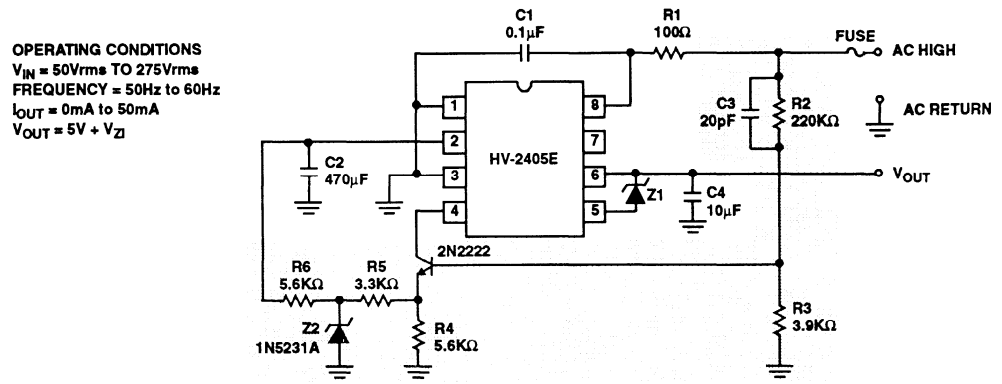
Unless Otherwise Specified: V_{IN} = 264Vms at 50Hz, C1 = 0.05µF, C2 = 470µF, C4 = 1µF, V_{OUT} = 5V, I_{OUT} = 50mA, Source Impedance R_1 = 150Ω. Parameters are Guaranteed at the Specific V_{IN} and Frequency Conditions, Unless Otherwise Specified. See test circuit for Component Location.

PARAMETER	CONDITIONS	TEMP	HV-2405E-5/-9			UNITS
			MIN	TYP	MAX	
Output Voltage (At Preset 5V)	V_{REF} = 0V_{DC}	+25°C	4.75	5.0	5.25	V
		Full	4.65	5.0	5.35	V
Output Voltage (At Preset 24V)	V_{REF} = 19V_{DC}	+25°C	22.8	24.0	25.2	V
		Full	22.32	24.0	25.68	V
Line Regulation	80Vrms to 264Vrms	+25°C	-	10	20	mV
		Full	-	15	40	mV
Load Regulation	(I_{OUT} = 5mA to 50mA)	+25°C	-	-	20	mV
		Full	-	-	40	mV
Output Current		Full	50	-	-	mA
Output Ripple (Vp-p)		Full	-	24	-	mV
Short Circuit Current Limit		Full	-	70	-	mA
Output Voltage TC		Full	-	0.02	-	%/°C
Quiescent Current Post Regulator	11V_{DC} to 30V_{DC} on Pin 2	+25°C	-	2	-	mA

Test Circuit



Application Information



COMPONENT LIST

FUSE = 1/ 4A	C1 = 0.1µF, AC RATED
R1 = 100Ω, 5W	C2 = 470µF, 15V + V_{OUT}, ELECTROLYTIC
R2 = 220kΩ, 1W	C3 = 20pF, CERAMIC
R3 = 3.9kΩ, 1/4W	C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
R4 = 5.6kΩ, 1/ 4W	Z1 = V_{OUT} - 5V, 1/4W
R5 = 3.3Ω, 1/ 4W	Z2 = 5.1V, 1N5231/A OR EQUIVALENT
R6 = 5.6kΩ, 1/4 W	Q1 = 2N2222 OR EQUIVALENT

FIGURE 1. OFF LINE WORLD-WIDE SUPPLY ($I_{OUT} \geq$ 50mA)

Off line World Wide Supply ($I_{OUT} \leq$ 50mA)

Figure 1 shows the recommended application circuit for an off line world wide supply. The circuit will deliver an output voltage of 5V to 24V and an output current from 0 to 50mA. The value of C2 can be reduced for applications requiring less output current (see section titled "Optimizing Design" for details). For a basic understanding of the internal operation of the HV-2405E reference section titled "How the HV-2405E Works".

The following is a detailed explanation of this application circuit:

Basic Operation:

When the input voltage goes positive an internal switch connects pin8 to pin2 allowing current to flow through R1 to charge up C2. When the voltage on C2 reaches a predetermined voltage the switch opens and the charging of C2 stops. R1 limits the input current and along with C1 provides a snubber for the internal switch. A linear regulator takes current from C2 further regulating the voltage and limiting the ripple at pin6. The voltage at pin6 is equal to V_{Z1} + 5V. The linear regulator also provides output current limiting. The capacitor C4 on pin6 is required for stability of the output.

Input Current Limiting Circuit

The external components in the shaded area of Figure 1 perform two functions. The first is to shut down the HV-2405E in the presences of a large voltage transients and the second is to provide input current limiting.

Resistors R2, R3 and capacitor C3 monitor the input voltage and turn on Q1 which shuts down the HV-2405E when the input voltage or the dv/dt is too large. This network anticipates the voltage applied to pin8, since R1 and C1 add several micro seconds delay, and turns off the HV-2405E when a predetermined input voltage is exceeded. The difference between R3/C3 and R1/C1 time constants ensures that the HV-2405E internal switch opens before the voltage, and thereby the input current, is allowed to rise to a dangerous level at pin 8.The input voltage at which the HV-2405E is turned off, is dependent upon the voltage on C2. The higher the voltage on C2 the larger the input current that the HV-2405E can safely turn off. For a detailed explanation of why the voltage on C2 determines the maximum input current that the HV-2405E can safely turn off, reference "Start-up" in section titled "How the HV-2405E Works".

Input current limiting is provided when the voltage at the base of Q1 forward biases the base to emitter junction, turning off the internal switch. The voltage required at the base to turn on Q1 increases as the voltage on C2 increases the emitter voltage. When the voltage on C2 is >10V, the emitter voltage is held constant by Z2 and the maximum input current is set by resistors R2, R3, R4 and R5 (see section titled "Design Equations" for more details).

Operation:

The circuit in Figure 1 ensures operation within the SOA of the HV-2405E by limiting the input current to <500mA when the voltage on C2 equals zero and <2A when the voltage on

Application Information (Continued)

C2 is greater than 10V. The circuits operation is illustrated in Figures 2 and 3. In Figure 2 the initial current pulse is approximately 400mA when V_{C2} = 0V and gradually increases to approximately 1.8A when C2 = 10V. Also notice that after the 17th line cycle the input current is approximately 1.4A. At this point C2 is fully charged. The input current required to maintain the voltage on C2 is less than the current to charge it and the circuit has reached steady state operation. Since the steady state current is less than the input current limit, the circuit in the shaded area is off and no longer has any effect.

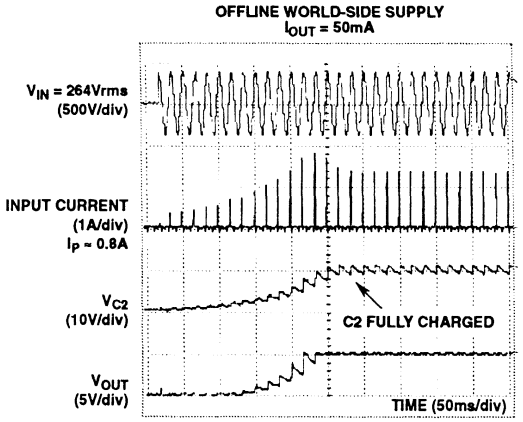


FIGURE 2. START UP OPERATION

Under short circuit operation the maximum voltage on pin 2 is less than 10V and the input current limiting circuit is invoked. Figure 3 shows that under output short circuit conditions, the input current is limited to about 800mA. The effects on the output current when the input current limiting circuit is invoked is illustrated in Figure 6.

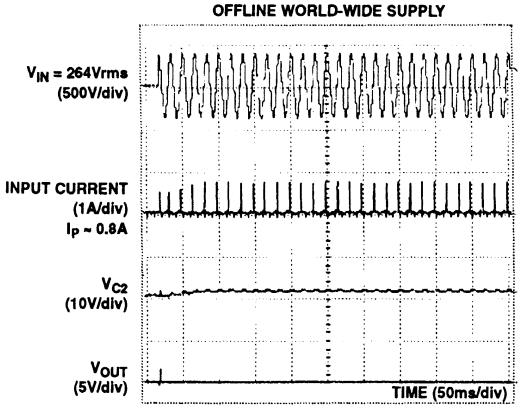


FIGURE 3. SHORT CIRCUIT OPERATION

Design Equations for Input Current Limiting

Initial Start-Up

Assume: V_{C2} = 0V, R1 = 100Ω, R2 = 220kΩ, R3 = 3.9kΩ, R4 = 5.6kΩ, R5 = 3.3kΩ, R6 = 5.6kΩ, V_{BE} = 0.54V, I_{TRIG} = 60µA, V_{Pin8} - V_{Pin2} = 3.5V @ low inputs currents. V_{IN1} = Voltage on AC high when input current limit circuit is invoked (V_{C2} = 0V)

$$I_{IN(min)} = \frac{V_{IN1} - V_{Pin8} - V_{Pin2}}{R1} \quad \text{(EQ 1)}$$

$$V_{IN1} = \frac{R2 + R3}{R3}\left(V_{BE} + \frac{R4\,(R5 + R6)}{R4 + R5 + R6} \times I_{TRIG}\right) \quad \text{(EQ 2)}$$

$$V_{IN1} = 57.41\,(0.54 + 3.437k\Omega \times 60\mu A) = 42.84V \quad \text{(EQ 3)}$$

$$I_{IN(min)} = \frac{42.84 - 3.5}{100} = 393mA \quad \text{(EQ 4)}$$

Equations 1 through 4, for the given assumptions, predict that the initial input current will be limited to 393mA.

The following equations can be used to predict the maximum input current during start-up.

Assume: V_{C2} > 10V, R1 = 100Ω, R2 = 220kΩ, R3 = 3.9kΩ, R4 = 5.6kΩ, R5 = 5.6kΩ, R6 = 3.3kΩ, V_{BE} = 0.54V, I_{TRIG} = 60µA, V_Z = 5.1V, V_{Pin8} - V_{Pin2} = 6V@ high inputs currents, V_{Pin2} - V_{Pin6}, V_{IN2} = Voltage on AC high when input current circuit is invoked (V_{C2} > 10V).

$$I_{IN(max)} = \frac{V_{IN2} - V_{OUT} - (V_{Pin8} - V_{Pin2}) - (V_{Pin2} - V_{Pin6})}{R1} \quad \text{(EQ 5)}$$

$$V_{IN2} = \frac{R2 + R3}{R3}\left[(V_{BE} + \frac{R4\,R5}{R4 + R5} \times I_{TRIG} + \frac{R4}{R4 + R5}V_{Z2}\right] \quad \text{(EQ 6)}$$

$$V_{IN2} = 57.41\,[0.54 + (2.076k\Omega \times 60\mu A) + (0.6292 \times 5.1)] \quad \text{(EQ 7)}$$

$$I_{IN(max)} = \frac{222 - V_{OUT} - 6 - 6}{100} = 2.05A\ @\ V_{OUT} = 5V \quad \text{(EQ 8)}$$

$$I_{IN(max)} = \frac{222 - V_{OUT} - 6 - 6}{100} = 1.86A\ @\ V_{OUT} = 24V \quad \text{(EQ 9)}$$

Equations 5 through 9 predict the maximum input current will be limited to less than 2.05A. In practice at 5 volt operation the current is less than predicted due to the low bias current through Z2.

Setting The Output Voltage

The circuit shown in Figure 1 provides a regulated 5V to 24V DC and is set by adjusting the value of Z1. The output voltage of the HV-2405E (pin6) is set by feedback to the sense pin (pin5). The output will rise to the voltage necessary to keep the sense pin at 5V. The output voltage is equal to the Zener voltage (V_{Z1}) plus the 5 volts on the sense pin. For a 5V output, pins 5 and 6 would be shorted together. The output voltage has the accuracy and tolerance of both the Zener diode and the band-gap of the HV-2405E (see Figure 16). The maximum output voltage is limited by Z_{B2} to ≈ $34V_{DC}$. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. Note: the output voltage can also be set by placing a resistor (1/4 watt) between pins 5 and 6. If a resistor is placed between pins 5 and 6 an additional 1 volt per kΩ (±10%) is added to the 5V output.

Application Information (Continued)

Optimizing Design (World-Wide Supply)

Selecting the Storage Capacitor C2:

For applications requiring less than 50mA or the full input voltage range, the value of C2 can be reduced for a more cost effective solution. The minimum C2 capacitor value is determined by the intersection between the maximum input voltage and the output current curve in Figure 4. (Note, for 50Hz operation see Figure 19 in section titled "Typical Performance Curves".) Advantages of making C2 as small as possible are:

- Reduced total size and cost of the circuit.
- Reduced start up time.

Consideration should be given to the tolerance and temperature coefficient of the C2 value selected. (Note; momentary peak output current demands should be considered in the sizing of C2. Increasing the output capacitor C4 is another way to supply momentary peak current demands.)

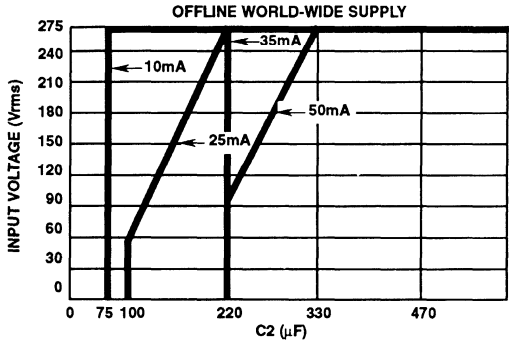


FIGURE 4. MINIMUM C2 VALUE vs INPUT VOLTAGE

The following example illustrates the method for determining the minimum C2 value required:

EXAMPLE

Requirements: V_{OUT} = 5V to 24V, I_{OUT} = 35mA, $V_{IN(max)}$ = 120Vrms, 60Hz.

For the given conditions, the minimum C2 value (from Figure 4) is determined to be 220µF.

Determining the Power Dissipation in R1:

Circuit efficiency is limited by the power dissipation in R1. The power dissipation for 240Vrms and 120Vrms is shown in Figure 5.

For input voltages other than 240Vrms or 120Vrms equation 10 can be used to determine the power dissipation in R1.

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad \text{(EQ 10)}$$

Example: R_1 = 100Ω, Input Voltage = 240Vrms, I_{OUT} = 50mA, P_D = 4.8W

NOTE: Under short circuit conditions the P_D in R1 decreases to 1.2W Due to fold back current limiting (I_{OUT} = 20mA, Reference Figure 6).

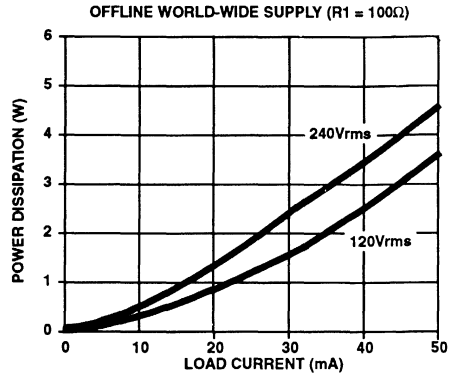


FIGURE 5. POWER DISSIPATION IN R1 vs LOAD CURRENT

Operation Information

Effects of Temperature on Output Current:

Figure 6 shows the effects of temperature on the output current for the circuit shown in Figure 1. Figure 6 illustrates operation with the output configured for 5V. Temperature effects on the output current for V_{OUT} = 24V operation is similar. The foldback current limiting is the result of reduced voltage on C2. The circuit delivers 50mA output current across the specified temperature range of -40°C to +85°C for all output voltages between 5V and 24V. The effect of decreasing the value of C2 (470µF) reduces the maximum output current (i.e. moves curve to the left). For all C2 values selected from Figure 4 (assuming tolerance and temperature coefficient are taken into account) the circuit meets the expected output current across the above mentioned temperature range.

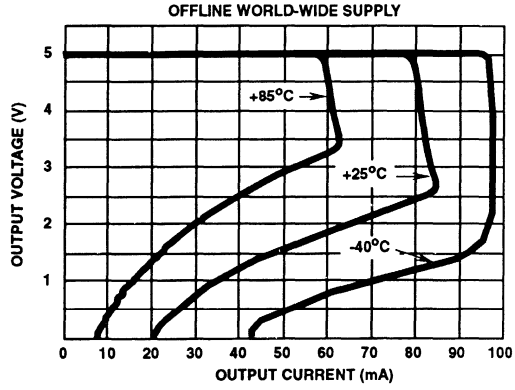


FIGURE 6. OUTPUT CURRENT vs TEMPERATURE

Application Information (Continued)

Minimum Input Voltage vs I_{OUT}

Table 1 shows the minimum input voltage range as a function of output current. Notice that the HV-2405E can deliver 5V at 10mA from a source voltage as little as 15Vrms and requires a minimum of 50Vrms to deliver 24V at 50mA.

TABLE 1. MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

V_{OUT} \ I_{OUT}	10mA	25mA	35mA	50mA
5V	15Vrms	21Vrms	25Vrms	30Vrms
24V	31Vrms	38Vrms	41Vrms	50Vrms

Component List (World Wide Supply <50mA)

Fuse

Opens the connection to the power line.

Recommended value: 1/4AG

R1 Source Resistor

R1 limits the input current into the HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. The maximum inrush current needs to be limited to less than 2A (V peak / R1 <2A). The equation for power dissipation in R1 is:

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad (EQ10)$$

Wirewound resistors are recommended due to their superior temperature characteristics.

R1 = 100Ω (±10%)

R2, R3, R4, R5 and R6 Resistors

R2, R3, R4, R5 and R6 set the bias level for Q1 that establishes the minimum and maximum input current limit during start-up.

Resistor values (±5%):

R2 = 220kΩ, 1W
R3 = 3.9kΩ, 1/4W
R4 = 5.6kΩ, 1/4W
R5 = 3.3kΩ, 1/4W
R6 = 5.6kΩ, 1/4W

C1 Snubber Capacitor

C1 and R1 form a low pass filter that limits the voltage rate of rise across SA1 (the main current carrying SCR of the HV-2405E) and therefore its power dissipation.

C1 = 0.1µF (±10%) AC rated, metallized polyester.

C2 Pre-Regulator Capacitor

C2 is charged once each line cycle. The post regulator section of the HV-2405E is powered by C2 for most of the line cycle. If the application requires a smaller input voltage, the value of C2 can be reduced from that shown in Figure 1 (see section on "Optimizing Design" for details). Note: capacitors with high ESR may not store enough charge to maintain full load current. The voltage rating of C2 should be about 10V greater than the selected V_{OUT}.

Recommended value = 470µF electrolytic (±20%), unless otherwise specified.

C3 Feed Forward Capacitor

C3 is part of the input Current limiting circuitry shown in Figure 1. C3 detects large voltage transients on the AC line and turns off the HV-2405E by turning Q1 on.

C3 = 20pF (20%), breakdown voltage >500V.

C4 Output Filter Capacitor

C4 is required to maintain the stability of the output stage. Larger values may help in supplying short momentary current peaks to the load and improve output ripple during start-up.

C4 = 10µF (±20%)

Z1 Output Voltage Adjust

Z1 is used to set the output voltage above the 5V reference on pin 5 (see section titled "Setting The Output Voltage" for more details).

Z1= V_{OUT} - 5V, 1/4 watt. V2 valve at 1mA.

Note, the wattage rating is different when configured as a dual supply (see dual supply section for on how to determine wattage).

Z2 Clamp Diode

Z2 clamps the voltage on Q1's emitter when the voltage on C2 >10V. This results in limiting the maximum input current to less than 2A.

Z2 = 5.1V, 1N5231A or equivalent

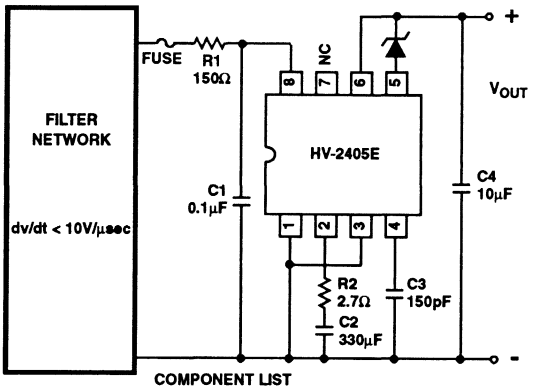
Q1 Input Current Limiting Transistor

Q1 shuts down the HV-2405E when the input voltage or dv/dt is too large.

V_{CEO} = 40V min.

Q1 = 2N2222 or equivalent

Imbedded Supply (I_{OUT} ≤30mA)



COMPONENT LIST

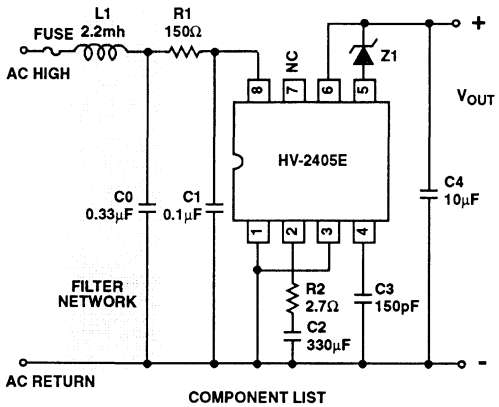
FUSE = 1/4A
R1 = 150Ω, 3W
R2 = 2.7Ω, 1/4W
C1 = 0.1µF, AC RATED
C2 = 330µF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 150pF, CERAMIC
C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
Z1 = V_{OUT} -5V, 1/4W

FIGURE 7. IMBEDDED SUPPLY I_{OUT} ≤ 30mA

Application Information (Continued)

For applications requiring 30mA or less and not directly off line (i.e. filter network preceding supply), the external transistor and associated resistors in Figure 1 can be replaced with a single 1/4 watt resistor R2 and capacitor C3 (Figure 7) if: (1) The filter network reduces the input dv/dt to less than 10V/µsec (ensures sufficient pin2 voltage at turn off), (2) Source resistor R1 equals 150Ω (limits the maximum input current) and (3) Inhibit Capacitor C3 equals 150pF (turns off the HV-2405E during large voltage transients).

For applications where EMI (conductive interference) is a design requirement, the circuit shown in Figure 8 is the recommended application circuit. This circuit delivers an output voltage of 5V to 24V with an output current from 0 to 30mA and passes VDE 0871 class "B" test requirements for conductive interference with a resistive load.



COMPONENT LIST

FUSE = 1/ 4A	C3 = 150pF, CERAMIC
R1 = 150Ω, 3W	C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
R2 = 2.7Ω, 1/4W	Z1 = V_{OUT} -5V, 1/4W
C1 = 0.1µF, AC RATED	L1 = 2.2mh, µ = 2000
C2 = 330µF, 15V + V_{OUT}, ELECTROLYTIC	C0 = 0.33µF, AC RATED

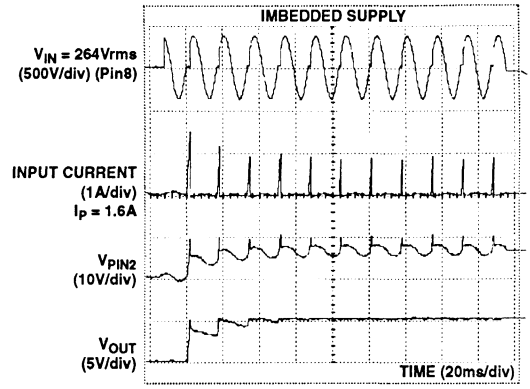
FIGURE 8. IMBEDDED SUPPLY WITH EMI FILTER ($I_{OUT} \leq 30mA$)

Basic Operation:

When power is initially applied the filter network reduces the magnitude of any transient noise spikes that might result in operation outside the SOA of the HV-2405E (see Start-up in section titled "How the HV-2405E Works" for and explanation of the SOA). When the voltage on pin 8 goes positive an internal switch connects pin8 to pin2 and C2 starts to charge through R1 and R2. When the voltage on pin2 reaches a predetermined voltage the switch opens and the charging of C2 stops. R1 limits the input current and along with C1 provides a snubber for the internal switch. R2 also has the effect of limiting the input current by increasing the voltage on pin2 sooner in the cycle. A linear regulator takes current from C2 and provides a DC voltage at pin6. The voltage at pin6 is equal to V_{Z1}+ 5V. The inhibit capacitor (C3) provides protection from large input voltage transients by turning off the HV-2405E and the output capacitor C4 provides stabilization of the output stage.

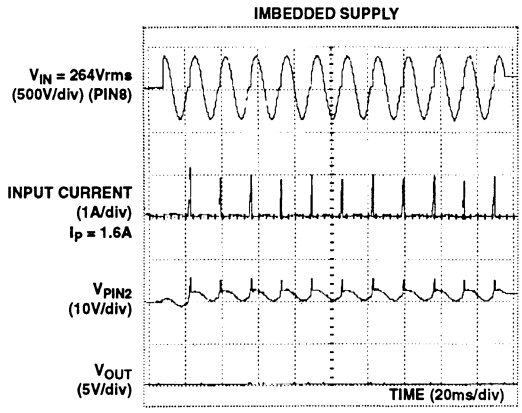
Operation:

The operation of the imbedded supply is illustrated in Figures 9 and 10. Figure 9 shows operation with a 30mA load and Figure 10 with the output short circuited. Notice that In both cases, the inhibit function of the HV-2405E prevents the circuit from turning on when the input voltage was applied near the peak line voltage. Also notice the initial current pulse (Figure 9) is approximately 1.6A and decreased to 1A within 40ms. This decrease in the input current results when the charging current required to maintain the voltage on C2 decreased. The effect of the series resistor (R2) is illustrated by the small voltage spike on the Vpin2 trace. This voltage spike increases the voltage on pin2 to the 10V trip point sooner in the cycle, thereby limiting the input current.



I_{OUT} = 30mA, V_{OUT} = 5V

FIGURE 9. START UP OPERATION



OUTPUT SHORT CIRCUITED

FIGURE 10. SHORT CIRCUIT OPERATION

Application Information (Continued)

Setting The Output Voltage

The circuits shown in Figures 7 and 8 provide a regulated 5V to 24V DC output voltage that is set by adjusting the value of Z1. The output voltage of the HV-2405E (pin 6) is set by feedback to the sense pin (pin5). The output will rise to the voltage necessary to keep the sense pin at 5V. The output voltage is equal to the Zener voltage (V_{Z1}) plus the 5 volts on the sense pin. For a 5V output, pins 5 and 6 would be shorted together. The output voltage has the accuracy and tolerance of both the Zener diode and the band-gap of the HV-2405E (see Figure 16). The maximum output voltage is limited by Z_{B2} to $\approx 34V_{DC}$. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. Note: the output voltage can also be set by placing a resistor (1/4 watt) between pins 5 and 6. If a resistor is placed between pins 5 and 6 an additional 1 volt per kΩ (±10%) is added to the 5V output.

Optimizing Design (Imbedded Supply)

Selecting the storage capacitor C2:

For applications requiring less than 30mA, the value of C2 can be reduced for a more cost effective solution. The minimum C2 capacitor value vs. output current is presented in Table 2. Advantages of making C2 as small as possible are:

- Reduced total size and cost of the circuit.
- Reduced start up time.

Consideration should be given to the tolerance and temperature coefficient of the C2 value selected. (Note: momentary peak output current demands should be considered in the sizing of C2. Increasing the output capacitor C4 is another way to supply momentary peak current demands.)

TABLE 2. IMBEDDED SUPPLY

R1 - 150Ω		R2 = 2.7Ω	
V_{IN}	FREQ.	C2	I_{OUT}
264Vrms	50Hz	330µF	30mA
		220µF	24mA
		100µF	14mA
		50µF	8mA
264Vrms	60Hz	330µF	30mA
		220µF	27mA
		100µF	16mA
		50µF	9mA
132Vrms	50Hz	330µF	30mA
		220µF	30mA
		100µF	16mA
		50µF	8mA
132Vrms	60Hz	330µF	30mA
		220µF	30mA
		100µF	16mA
		50µF	9mA

Determining the Power Dissipation in R1:

Circuit efficiency is limited by the power dissipation in R1. The power dissipation for 240Vrms and 120Vrms is shown in Figure 11.

For input voltages other than 240Vrms or 120Vrms equation 10 can be used to determine the power dissipation in R1.

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad \text{(EQ 10)}$$

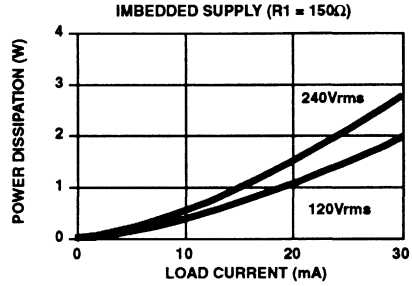


FIGURE 11. POWER DISSIPATION IN R1 vs LOAD CURRENT

Operation information

Effects of Temperature on Output Current:

Figures 12 and 13 show the effects of temperature on the output current for the imbedded supply (R2 = 2.7Ω). Figure 12 illustrates V_{OUT} = 5V operation and Figure 13 illustrates V_{OUT} = 24V operation. The imbedded supply (R2 = 2.7Ω) delivers 30mA output current across the specified temperature range of -40°C to +85°C for all output voltages between 5V and 24V. The effect of decreasing the value of C2 (330µF) reduces the maximum output current (i.e. moves curve to the left). For all C2 values selected from Table 2 (assuming tolerance and temperature coefficient are taken into account) the circuit meets the expected output current across the above mentioned temperature range.

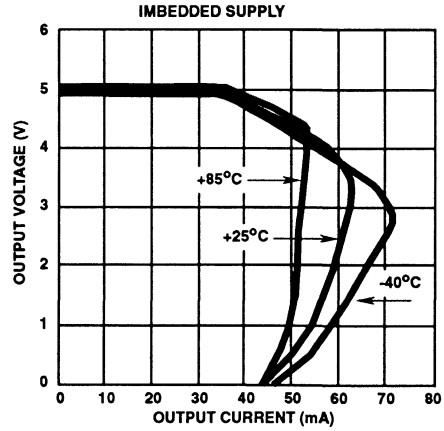


FIGURE 12. OUTPUT CURRENT vs TEMPERATURE (R1 = 150Ω, R2 = 2.7Ω, C2 = 330µF)

Application Information (Continued)

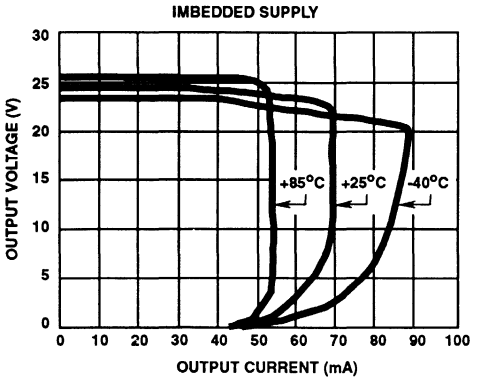


FIGURE 13. OUTPUT CURRENT vs TEMPERATURE (R1 = 150Ω, R2 = 2.7Ω, C2 = 330μF)

Component List (Imbedded Supply ≤30mA)

Fuse

Opens the connection to the power line should the system fail.

Recommended value: 1/4AG

R1 Source Resistor.

R1 limits the input current into the HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. The maximum inrush current needs to be limited to less than 2A (Vpeak / R1 < 2A). The equation for power dissipation in R1 is:

$$Pd = 2.8\ \sqrt{R1\ Vrms\ (I_{OUT})^3}$$

Wirewound resistors are recommended due to their superior temperature characteristics.

R1 = 150Ω (±10%)

R2 Series Resistor

R2 limits the input current by boosting the voltage on pin 2 sooner in the cycle.

R2 = 2.7Ω (5%), 1/4 Watt

C1 Snubber Capacitor

C1 and R1 form a low pass filter that limits the voltage rate of rise across SA1 (the main current carrying SCR of the HV-2405E) and therefore its power dissipation.

C1 = 0.1μF (±10%) AC rated, metallized polyester.

C2 Pre-Regulator Capacitor

C2 is charged once each line cycle. The post regulator section of the HV-2405E is powered by C2 for most of the line cycle. If the application requires a smaller input voltage, the value of C2 can be reduced from that shown in Figures 7 or 8 (see section on "Optimizing Design" for details. Note; capacitors with high ESR may not store enough charge to maintain full load current. The voltage rating of C2 should be about 10V greater than the selected V_{OUT}.

Recommended value = 330μF electrolytic (±20%),unless otherwise specified.

C3 Inhibit Capacitor

C3 keeps the HV-2405E from turning on during large input voltage transients.

C3 = 150pF (10%)

C4 Output Filter Capacitor

C4 is required to maintain the stability of the output stage. Larger values may help in supplying short momentary current peaks to the load and improves output ripple during start-up.

C4 = 10μF (±20%)

Z1 Output Voltage Adjust

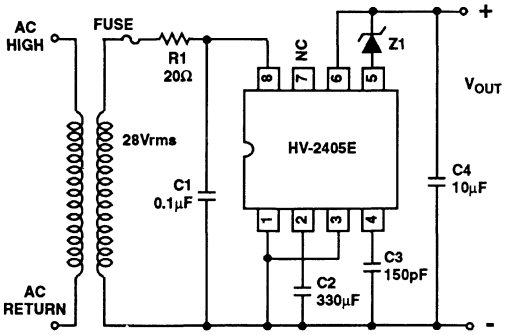
Z1 is used to set the output voltage above the 5V reference on pin 5 (see section titled "Setting The Output Voltage" for more details).

Z1 = V_{OUT} - 5V,1/4 watt.

Note, the wattage rating is different when configured as a dual supply (see dual supply section for on how to determine wattage).

Low Input Voltage Supply (I_{OUT} <50mA)

An ideal application, taking advantage of the low voltage operation, would be thermostat controls were 28Vrms is supplied via a transformer. In this application the HV-2405E could deliver a regulated 5V at 40mA with a power dissipation in R1 (R1= 20Ω) equal to 530mw. The current limiting components, in Figure 1, are not required at this low input voltage level. See Figures 23 and 24 for output vs. temperature.



COMPONENT LIST

FUSE = 1/ 4A, OPTIONAL	C2 = 470μF, 15V + V_{OUT}, ELECTROLYTIC
R1 = 20Ω, 1W	C3 = 150pF, CERAMIC
R2 = 2.7Ω, 1/4W	C4 = 10μF, V_{OUT} + 10V, ELECTROLYTIC
C1 = 0.05μF, AC RATED	Z1 = V_{OUT} -5V, 1/4W

FIGURE 14. LOW INPUT VOLTAGE SUPPLY

Application Information (Continued)

COMPONENT LIST

FUSE = 1/ 2A
R1 = 100Ω, 5W
R2 = 220kΩ, 1W
R3 = 3.9kΩ, 1W
R4 = 5.6kΩ, 1/ 4W
R5 = 3.3Ω, 1/ 4W
R6 = 5.6kΩ, 1/4 W
C1 = 0.1µF, AC RATED
C2 = 470µF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 20pF, CERAMIC
C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
Z1 = V_{OUT} - 5V, 1/4W
Z2 = 5.1V, 1N5231/A OR EQUIVALENT
Q1 = 2N2222 OR EQUIVALENT

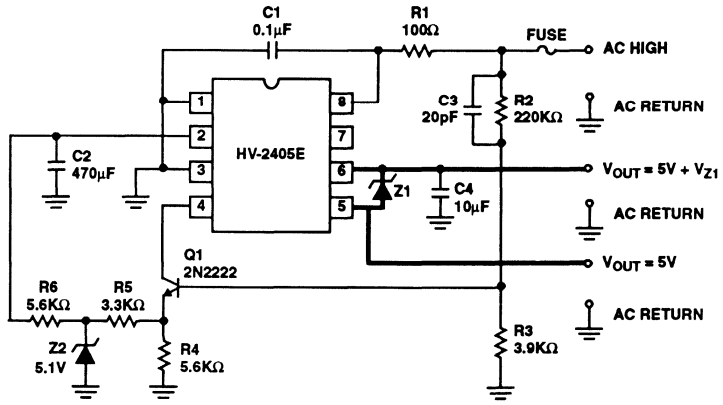


FIGURE 15. DUAL SUPPLY

Dual Supply (I_{OUT} <50mA)

Dual output voltages are available by making use of the 5 volt reference at pin 5. The sum of both supply currents must not exceed maximum output current limit of 50mA. The output current for the 5 volt supply is delivered from the output (pin 6) through the Zener diode. The wattage calculation for the Zener diode is given in Equation 11.

Wattage = (V pin 6 - V pin 5) (I_{OUT} pin 5) (EQ 11)

General Precautions

CAUTION: This product does not provide isolation from the AC line. Failure to use a properly rated fuse may cause R1 to reach dangerously high temperatures or cause the HV-2405E to crack or explode.

Instrumentation Effects:

Background:

Input to output parasitic exist in most test equipment power supplies. The inter-winding capacitance of the transformer may result in substantial current flow (mA) from the equipment ground wire to the AC and DC ground of the HV-2405E. This current can induce instability in the inhibit circuit of the HV-2405E resulting in erratic operation.

Recommendations for evaluation of the HV-2405E in the lab:

a). The use of battery powered DVM's and scopes will eliminate ground loops.

b). When connecting test equipment, locate grounds as close to pin 1 as possible.

c). Current measurements on the AC side of the HV-2405E (Pin 8, 1 and 2) should be made with a non-contact current probe.

If AC powered test equipment is used, then the use of an isolated plug is recommended. The isolated plug eliminates any voltage difference between earth ground and AC ground. However, even though the earth ground is disconnected, ground loop currents can still flow through transformer of the test equipment. Ground loops can be minimized by connecting the test equipment ground probe as close to pin 1 as possible.

Caution: Dangerous voltages may appear on exposed metal surfaces of AC powered test equipment.

AC Source Effects:

Background:

Laboratory AC sources (such as VARIACs, step-up transformers etc.) contain large inductances that can generate damaging high voltage transients any time they are switched on or off. Switch arcing can further aggravate the effects of source inductance.

Recommendation:

Adequate protection means (such as MOV, avalanche diode, surgector, etc.) may be needed to clamp transients to within the ±500V input limit of the HV-2405E.

Output Short Circuited:

For output voltages greater than 5V the maximum voltage rating from pin 2 to pin 6 (15V) could be exceeded. For a 24V output the voltage on pin 2 could be as high as 32V. Under normal operating conditions the voltage differential between pin2 and pin 6 is maintained by DA3, DA4, DA5 and ZA1 (Figure 6) to about 6V. However, if the output (pin6) is shorted to ground the potential difference would equal the voltage on C2 which would exceed the 15V max limit. (Note: if the output is shorted prior to initial power up, the voltage on C2 only reaches about 6.8V and therefore is not a problem.)

Recommendation:

If the possibility of the output being shorted to ground during normal operation exist, a 10V zener diode (cathode pin 2, anode pin 6) is recommended from pin 2 to pin 6.

Safe Operating Area

Ensure operation is within the SOA of the HV-2405E. Reference "Start-Up" in section titled "How the HV-2405E Works".

How The HV-2405E Works

Steady State Operation:

The HV-2405E converts an AC voltage into a regulated DC voltage. This is accomplished in two functional sections (1) Switching Pre-Regulator and (2) Linear Voltage Regulator. Refer to HV-2405E schematic Figure 16.

The purpose of the Switching Pre-Regulator circuit is to capture energy from an incoming AC power line, 1/6 of every positive half cycle and store this energy in an electrolytic capacitor (C2). This energy is then transferred to the Linear Voltage Regulator.The current path for charging C2 is through DA1, SA1 and DA2. When the voltage level on C2 reaches approximately 6.8V above the output voltage, SA2 turns on turning off SA1 and the charging of C2 stops until the next positive half cycle on AC high. SA2 is triggered on when current flows out of SA2's anode gate and through the Zener diode stack (ZA1, DA3, DA4, DA5). This results in a feedback circuit that limits the peak voltage on pin 2.

The input voltage and current wave forms at pin 8 are illustrated in Photo 1. The operation of the HV-2405E is easily confirmed by noticing the clamping of the input voltage during the charging of C2. Photo 2 shows the voltage on C2 (bottom trace), along with the voltage on pin 8 as a reference. The test conditions for the wave forms are listed at the end of this section.

The Linear Voltage Regulator performs two functions. The first is to provide a reference voltage at pin 5 that is temperature independent and the second is to provide an output voltage on pin 6 that is adjustable from 5 volts to 24 volts. The band-gap (NB1, NB2, RB3 and RB4) provides a temperature independent reference voltage on the base of NB5. This reference voltage (1.21V) results in approximately 1 mA through RB10 when the feedback loop from pin 6 is closed. The output voltage is adjusted by placing a Zener diode between pins 5 and 6. The output voltage on pin 6 is adjusted above the 5 volt reference on pin 5 by a value equal to the Zener voltage. The maximum output voltage is limited to $\approx 34V_{DC}$ by the internal Zener diode Z_{B2}. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. The bottom trace of Photo 3 shows the output voltage ripple (worst case conditions), along with the voltage on pin 8 as a reference.

Test conditions for waveforms: $T_A = +25°C$, $V_{AC} = 240Vrms$, f = 50Hz, R1 = 150Ω, C1= 0.1µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, $V_{OUT} = 5V$ @ 50mA.

Start-up:

Start up operation is similar to that described above. Since the storage capacitor connected to pin 2 is discharged, the main SCR, SA1, has to pass more current than for steady state.

The ability of the second SCR, SA2, to turn off SA1 is a function of the voltage on C2. Due to the impedances of SA1 and SA2, the maximum input current that can be safely turned off decreases for C2 voltages below 5V. To understand why the voltage on C2 determines the maximum input current that the HV-2405E can safely turn off, its important to understand the electrical connection between SA1, SA2 and the storage capacitor C2. Figure 17(a) is a schematic representation of both SCR'S and is presented to explain how SA2 turns off SA1.

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Current into Pin 8, (0.5A/Div)

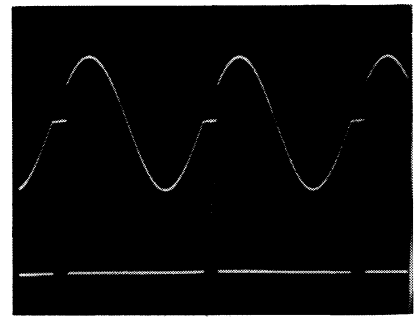


PHOTO 1

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Pre-Regulator Capacitor Voltage, C2 (5V/Div) @ Approximately 10V DC

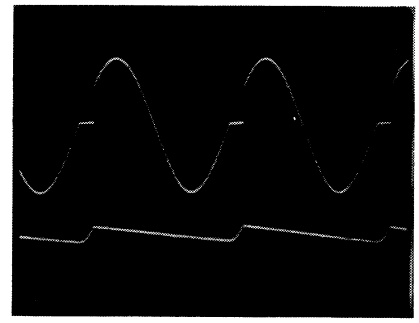


PHOTO 2

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Ripple or Switch Spike on Regulator 5V DC Output (50mV/Div) This is Worst Case Ripple (High Line Voltage, Maximum I_{OUT})

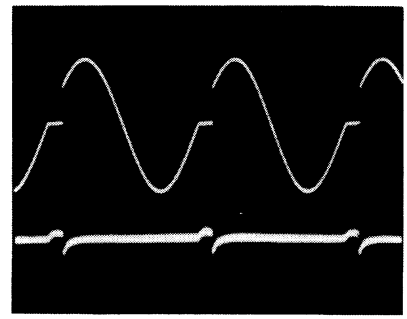


PHOTO 3

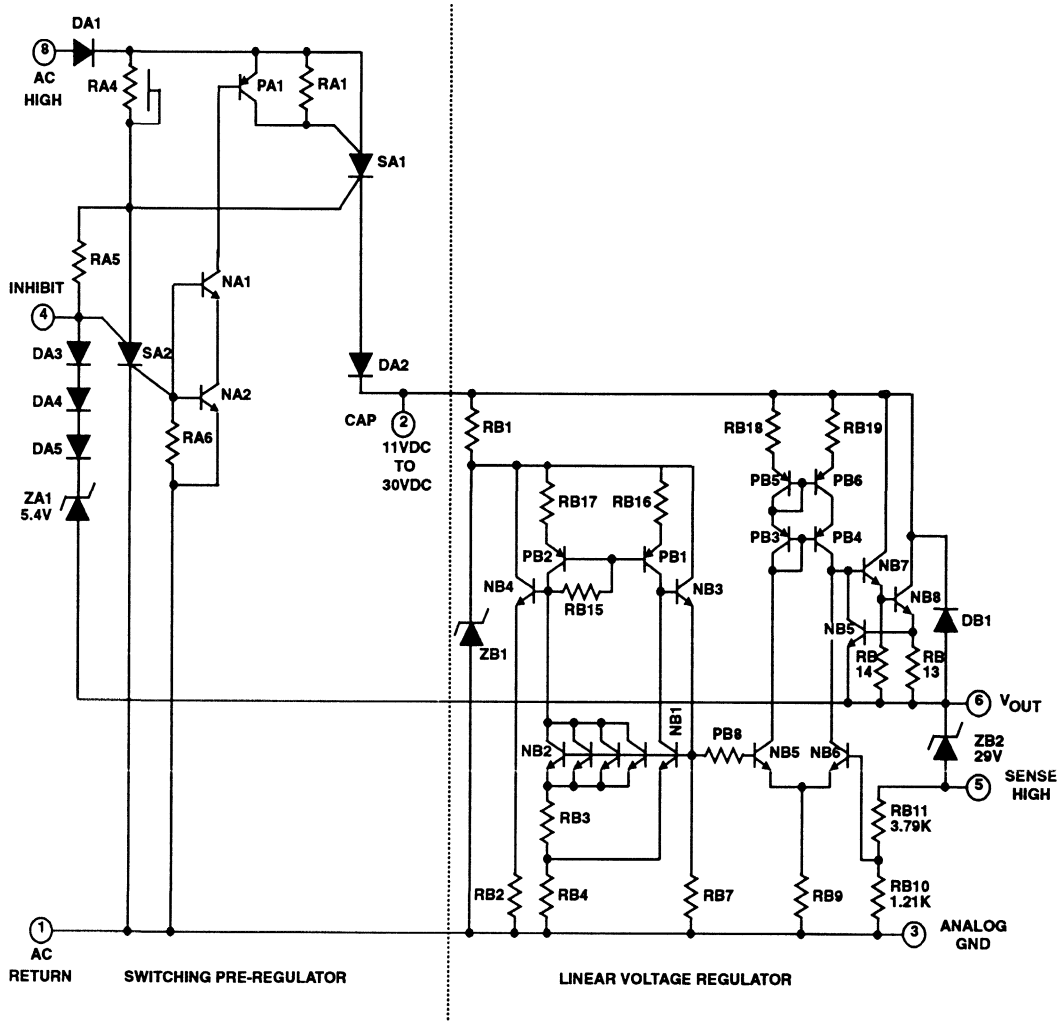


FIGURE 16. HV-2405E SCHEMATIC DIAGRAM

Assume that SA1 is on and the current path is from pin 8 to pin 2. If a small current is pulled out of the base of SA2's pnp (point 1, Figure 17a) SA2 will turn on. When SA2 turns on the collector current of SA1's pnp no longer provides base drive to its npn and SA1 turns off. Figure 17(b) shows the current relationships for both SCR's.

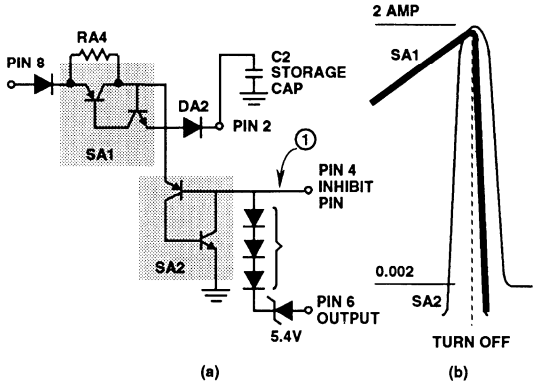


FIGURE 17 (a) (b). SCHEMATIC REPRESENTATION OF SCR's

In order for current to be pulled out of the base of SA2's pnp the voltage on the pnp's emitter will have to be more positive than the voltage on the base. The voltage on the base is referenced 7.5V above the output voltage by the zener diode stack between pins 4 and 6. When the voltage on pin 2 reaches 6.8V (7.5V-1Vbe) above the output voltage, current flows and SA2 is gated on. With 6.8 volts above the output voltage on C2, there is a sufficient voltage across SA2 to turn off SA1 by sinking 100% of SA1's anode current.

SA2 could be triggered on before C2's voltage is sufficient to ensure that SA2 can sink 100% of SA1's current, by noise on pin8. In this case SA1 goes into a high impedance state but does not turn off. This condition can exist if switch arcing triggers enough current through the inhibit capacitor to prematurely turn on SA2.

The **S**afe **O**perating **A**rea (SOA) of the HV-2405E is defined by the voltage on C2 and the magnitude of the input current. Figure 18 shows the safe operating area of the HV-2405E.

Under normal operating conditions the HV-2405E does not turn off the input current until the voltage on C2 is well above 5V. Input currents larger than the safe turn off value in Figure 10 do not present any problems as long as the HV-2405E does not attempt to interrupt them.

During start up operation, power line noise, typically generated by switch bounce/arcing, may accidently initiate input current turn off before C2 is charged. The application circuit shown in Figure 1 never permits the HV-2405E to operate outside the safe turn off current region so any false turn off signals have no effect. Also, once the capacitor is charged, noise causes no problems.

For applications where there is little noise during start up, the external transistor and associated resistors are not needed. A 150pF capacitor connected to pin 4 helps keep the HV-2405E turned off until any switching noise dies out. Also the input resistor R1 may have to be increased to limit the input current to the allowable maximum.

Some applications inherently have little start-up noise. EMI filters between the power switch and the HV-2405E greatly attenuate switch bounce noise. Likewise, the presences of large capacitors connected through bridge rectifiers act as filters. Solid-state relays that close at the line zero crossing generate little noise. Also, there is no problem if power is applied during the negative part of the line cycle. [The user is cautioned to verify the suitability of his application circuit. Contact Harris Applications for specific questions.]

If the safe turn off current is exceeded, SA1 will fail as a short circuit. However, SA2 will continue to act, temporarily, as shunt regulator to keep the voltage on pin 2 from exceeding the safe limit of the post regulator. The voltage at pin 6 will not change. Failure to use a properly rated fuse may cause R1 to reach dangerously high temperatures or cause the HV-2405E to crack or explode.

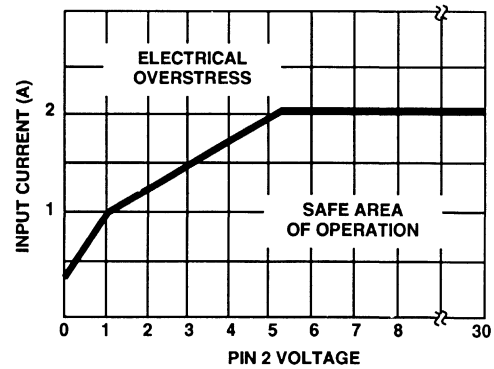


FIGURE 18. HV-2405E SAFE INTERRUPT CURRENT vs PIN 2 VOLTAGE

HV-2405E Waveforms

Unless Otherwise Specified: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V @ 50mA, 5ms/div.

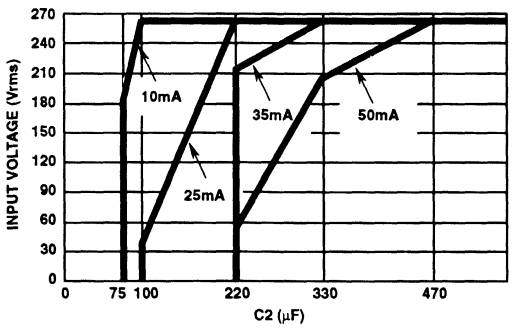


FIGURE 19. MINIMUM C2 VALUE vs INPUT VOLTAGE 50Hz

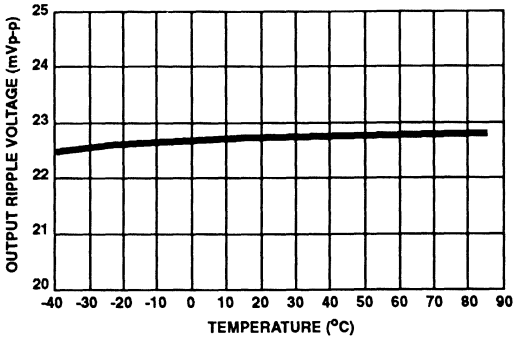


FIGURE 20. OUTPUT RIPPLE VOLTAGE vs TEMPERATURE

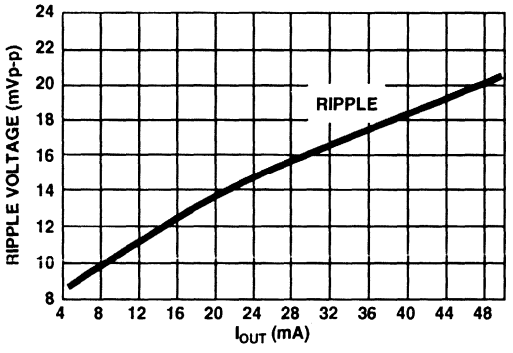


FIGURE 21. OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

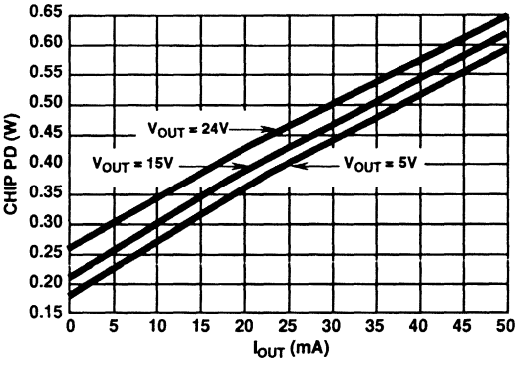


FIGURE 22. CHIP POWER DISSIPATION vs OUTPUT CURRENT

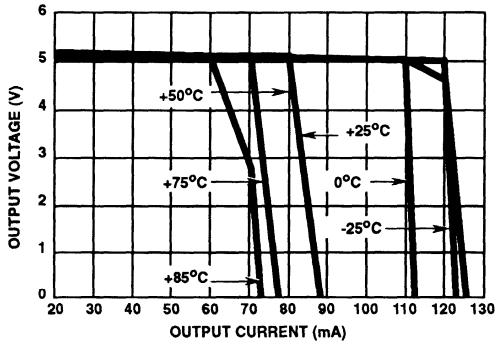


FIGURE 23. OUTPUT CURRENT LIMIT ($5V_{OUT}$) 50HZ
50mA is the Maximum Recommended Output Current

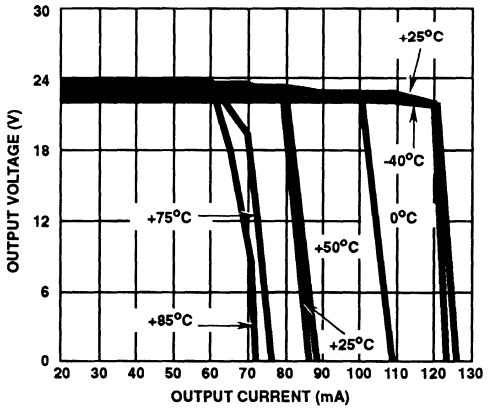


FIGURE 24. OUTPUT CURRENT LIMIT ($24V_{OUT}$) 50Hz
50mA is the Maximum Recommended Output Current

HARRIS SEMICONDUCTOR

CA3085, CA3085A CA3085B

Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA

October 1992

Features

- Up to 100mA Output Current
- Input and Output Short-Circuit Protection
- Load and Line Regulation 0.025%
- Pin Compatible with LM100 Series
- Adjustable Output Voltage

Applications

- Shunt Voltage Regulator
- Current Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Combination Positive and Negative Voltage Regulator
- Dual Tracking Regulator

TYPE	V_{IN} RANGE V	V_{OUT} RANGE V	MAX I_{OUT} mA	MAX LOAD REGULATION $\%V_{OUT}$
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

Description

The CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7V to 46V at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

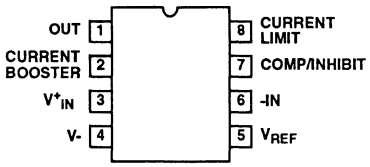
The CA3085A and CA3085B have output current capabilities up to 100mA and the CA3085 up to 12mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5V to 30V (CA3085), 7.5V to 40V (CA3085A), and 7.5V to 50V (CA3085B) and a minimum regulated output voltage of 26V (CA3085), 36V (CA3085A), and 46V (CA3085B).

Ordering Information

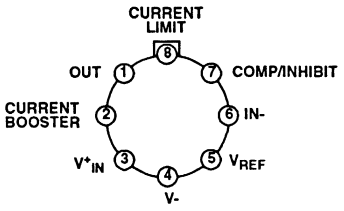
PART NUMBER	TEMPERATURE	PACKAGE
CA3085, A, B	-55°C to +125°C	8 Lead TO-5 Style
CA3085S, AS, BS	-55°C to +125°C	8 Lead TO-5 Dil-Can
CA3085E, AE, BE	-55°C to +125°C	8 Lead Plastic DIP
CA3085H	+25°C	Die Form

Pinouts

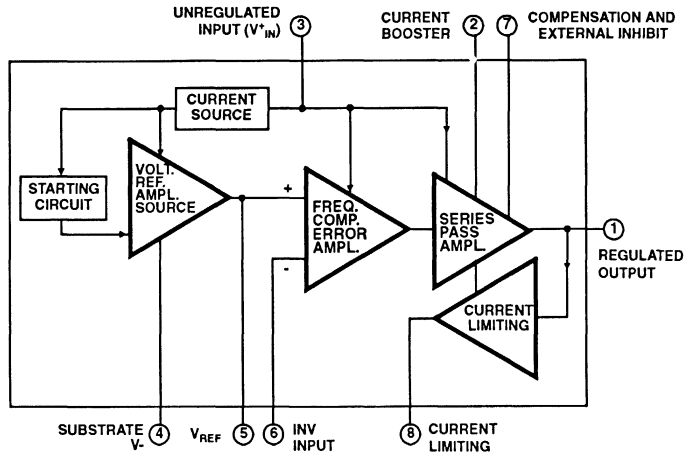
8 LEAD PLASTIC DIP
8 LEAD TO-5 DIL-CAN
TOP VIEW



8 LEAD TO-5 STYLE
TOP VIEW



Functional Block Diagram



HARRIS SEMICONDUCTOR

CA3169

Solenoid and Motor Driver (1/2 H Driver)

October 1992

Features

- Chip Encapsulated in a 5-Lead Plastic TO-220 Style Package
- Output Short Circuit Protection
- Thermal Overload Protection
- Solenoid Inductive "Kick" Protection with Internal-Clamp Diodes
- Output Sink and Source Capacity of 600mA Minimum Over Temperature
- Separate Sink Circuit and Source Circuit, Each Individually Controlled

Applications

- Latching Solenoid Driver (Single and Multiple)
- Non-Latching Solenoid Driver
- Relay Driver
- Lamp Controller
- Lamp Driver
- Motor Controller (Forward and Reverse)
- Stepper Motor Controller
- On-Off Logic Controllers (TTL Logic)
- Intermediate Power Driver
- Triac, SCR, and Transistor Drivers

Description

The CA3169 ia a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or nonlatching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source driver circuit with internal current limiting protection and a separate sink driver circuit. The sink driver contains an energy absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

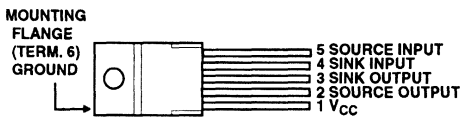
The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO.

Ordering Information

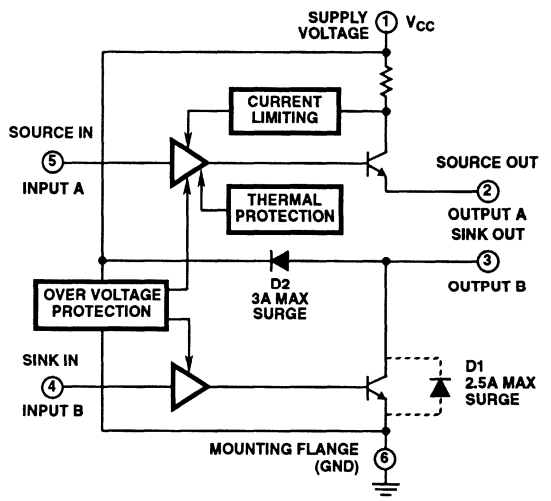
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3169	-40°C to +85°C	5 Lead Plastic SIP

Pinout

5 PIN PLASTIC SIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1277.3**

This page supersedes DB304 page 4-3

HARRIS SEMICONDUCTOR

HIP2500

October 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive N-Channel Power Devices
- Floating Bootstrap Power Supply for Upper Rail Drive
- CMOS Schmitt-Triggered Inputs with Hysteresis and Pull-Down
- 100kHz Operation
- Single Low Current Bias Supply
- Latch-up Immune CMOS Logic
- Peak Drive..... Up to 2.0A
- Gate Drive Switching Time ..... < 150ns Typ

Applications

- High Frequency Switch-Mode Power Supply
- Induction Heating and Welding
- Switch Mode Amplifiers
- AC and DC Motor Drives
- Electronic Lamp Ballasts
- Battery Chargers
- UPS Inverters

Description

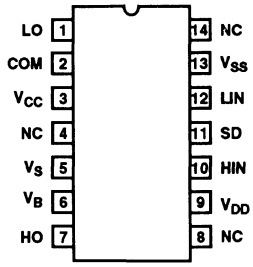
The HIP2500 is a high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control for PWM motor drive, power supply, and UPS applications.

Ordering Information

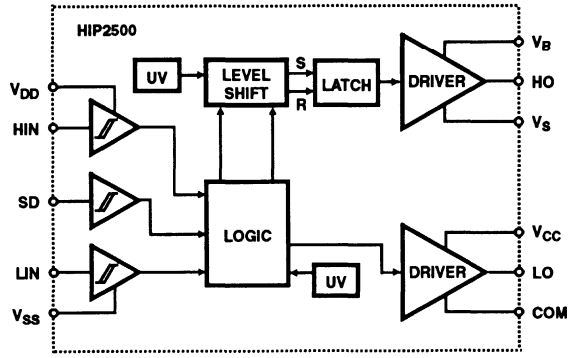
PART	TEMPERATURE	PACKAGE
HIP2500IP	-40°C to +85°C	14 Lead Plastic DIP

Pinout

14 PIN PLASTIC DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2801.3**

This page supersedes DB304 page 4-8

Absolute Maximum Ratings

Full Temperature Range Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Otherwise Noted.

Floating Supply Voltage, V_B . . . . . V_S-0.5V to V_S+18.0V
(Positive Terminal)
Floating Supply Voltage, V_S 500V
(Common Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . -0.5V to V_B+0.5V
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to 18.0V
Low Side Channel Output Voltage, V_{LO} . . . . . -0.5V to V_{CC}+0.5V
Logic Supply Voltage, V_{DD} . . . . . -0.5V to 18.0V
Logic Input Voltage, V_{IN} . . . . . -0.5V to V_{DD}+0.5V
[HIN, LIN & SD (Shutdown)]

Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package . . . . . 85°C/W
Maximum Package Power Dissipation at +85°C
Plastic DIP Package 470mW
Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C
Operating Ambient Temperature Range, T_A . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended DC Operating Conditions

Floating Supply Voltage, V_B . . . . . V_S+10V to V_S+15V
(Floating Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . 10V to V_B
(With Respect to V_S)
Fixed Supply Voltage, V_{CC} . . . . . 10V to 15V
Low Side Channel Output Voltage, VLO . . . . . 0V to V_{CC}
Logic Supply Voltage, V_{DD} . . . . . 4V to V_{CC}
Floating Supply Voltage, V_S . . . . . -4.0V to 500V
(Common Terminal)

Electrical Specifications

V_{CC} = (V_B-V_S) = V_{DD} = 15V, C_{OM} = V_{SS} = 0 and T_A = +25°C, Unless Otherwise Noted

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Quiescent V_{CC} Current	I_{QCC}	-	1.5	1.9	mA
Quiescent V_{BS} Current	I_{QBS}	-	300	400	µA
Quiescent V_{DD} Current	I_{QDD}	-	0.1	1	µA
Quiescent Leakage Current	I_S (500V)	-	0.4	3.0	µA
Logic Input Pulldown Current, V_{IN} = V_{DD} (HIN, LIN, SD)	IN+	-	12	20	µA
Logic Input Leakage Current, V_{IN} = V_{SS} (HIN, LIN, SD)	IN-	-	0	1	µA
Logic Input Positive Going Threshold	V_{TH}+	7.5	8.0	8.5	V
Logic Input Negative Going Threshold	V_{TH}-	5.5	5.9	6.3	V
Undervoltage Positive Going Threshold	UV+	8.0	9.35	9.99	V
Undervoltage Negative Going Threshold	UV-	7.7	9.05	9.69	V
Undervoltage Hysteresis (V_{CC})	UVHYS (V_{CC})	350	-	450	mV
Undervoltage Hysteresis (V_{BS})	UVHYS (V_{BS})	250	-	450	mV
Output High Open Circuit Voltage (HO, LO)	V_{OUT}+	14.95	15	-	V
Output Low Open Circuit Voltage (HO, LO)	V_{OUT}-	-	-	0.05	V
Output High Short Circuit Current (Sourcing)	I_{OUT}+	1.65	2.1	-	A
Output Low Short Circuit Current (Sinking)	I_{OUT}-	1.85	2.3	-	A

This page supersedes DB304 page 4-9

Switching Specifications

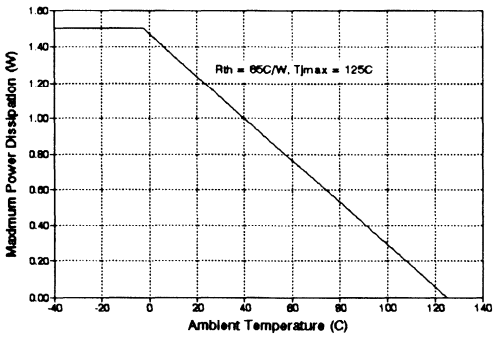
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
High Side Turn-On Propagation Delay	t_{ON}	320	420	525	ns
High Side Turn-Off Propagation Delay	t_{OFF}	300	385	450	ns
High Side Turn-On Rise Time	t_R	-	25	35	ns
High Side Turn-Off Fall Time	t_F	-	25	35	ns
LOW SIDE CHANNEL, CL = 1000pF					
Low Side Turn-on Propagation Delay	t_{ON}	250	365	450	ns
Low Side Turn-off Propagation Delay	t_{OFF}	225	295	370	ns
Low Side Turn-on Rise Time	t_R	-	25	35	ns
Low Side Turn-off Fall Time	t_F	-	25	35	ns
Shutdown Propagation Delay High Side Shutdown	t_{SDHO}	300	400	490	ns
Low Side Shutdown	t_{SDLO}	240	320	400	ns
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
Turn-On Propagation Delay Matching (Between HO and LO)	M_t	0	75	125	ns
Minimum On Output Pulse Width (HO, LO)	$PW_{OUT(MIN)}$	-	35	50	ns
Minimum Off Output Pulse Width (HO, LO)	$PW_{\overline{OUT}MIN}$	275	440	590	ns
Minimum Input Pulse Width (ON)	$PW_{ON(MIN)}$	-	100	145	ns
Minimum Input Pulse Width (OFF)	$PW_{OFF(MIN)}$	-	110	160	ns
Deadtime LO Turn-off to HO Turn-on	DHt_{ON}	95	125	155	ns
Deadtime HO Turn-off to LO Turn-on	DLt_{ON}	-50	-20	0	ns
MAXIMUM TRANSIENT CONDITIONS					
Offset Supply Operating Transient	dV_S/dt	-	-	50	V/ns

Logic Truth Table

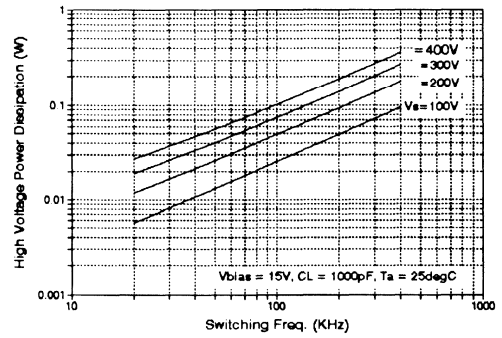
HIN	LIN	UV_H	UV_L	SD	HO	LO	COMMENTS
0	0	0	0	0	0	0	Normal Off
0	1	0	0	0	0	1	Lower On
1	0	0	0	0	1	0	Upper On
1	1	0	0	0	1	1	Both On
X	X	X	X	1	0	0	Chip Disabled
X	X	1	1	X	0	0	V_{CC} UV Lockout and V_{BS} Lockout
X	1	1	0	0	0	1	V_{BS} UV Lockout
1	X	0	1	0	1	0	V_{CC} UV Lockout

Performance Curves

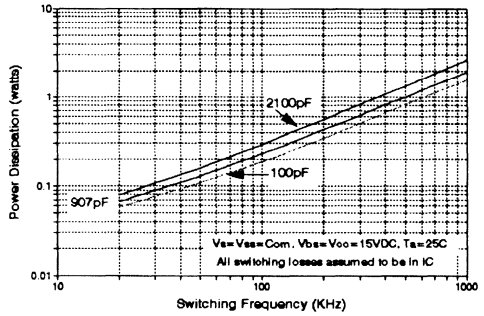
MAXIMUM POWER DISSIPATION vs TEMPERATURE



HIGH VOLT POWER DISSIPATION vs. SWITCHING FREQUENCY



LOW VOLTAGE POWER DISSIPATION vs FREQUENCY



HARRIS SEMICONDUCTOR

HIP4011

October 1992

Three-Phase Brushless DC Motor Controller

Features

- 3A DC, 5A Peak Output Current
- 16V Max. Rated Supply Voltage
- Built-in "Free-Wheeling" Diodes
- Output dv/dt Limited to Reduce EMI
- External Dynamic Brake Control Switch With Undervoltage Sense
- Thermal & Current Limiting Protects Against Locked Rotor Conditions
- Provides Analog Current Sense & Reference Inputs
- Decode Logic with Illegal Code Rejection

Applications

- Drive Spindle Motor Controller
- 3ϕ Brushless DC Motor Controller
- Brushless DC Motor Driver for 12V Battery Powered Appliances
- Phased Driver for 12V DC Applications
- Logic Controlled Driver for Solenoids, Relays & Lamps

Description

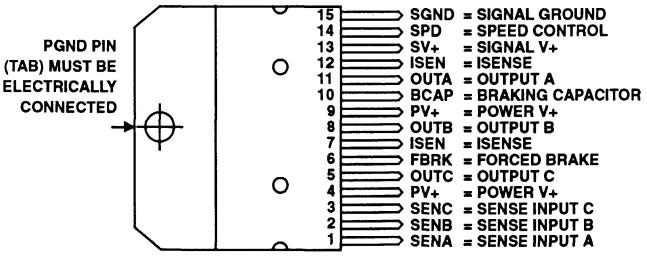
The HIP4011 motor driver is intended for three phase brushless motor control at continuous output currents up to 3A. It accepts inputs from buffered Hall effect sensors and drives three motor windings, regulating the current through an external current sensing resistor, according to an analog control input. Output "freewheeling" diodes are built in and output dv/dt is limited to decrease the generated EMI. Thermal and current limiting are used to protect the device from locked rotor conditions. A brake control input forces all outputs to ground simultaneously to provide dynamic braking, and an internal voltage sensor does the same when the supply drops below a predetermined switch point. Power down braking energy is stored in an external capacitor.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4011IS	-40°C to +85°C	15 Pin Plastic SIP Surface Mount

Pinout

15 LEAD PLASTIC SIP
TOP VIEW



OUTPUT TRUTH TABLE

SENSOR INPUTS			FORCE BRAKE INPUT*	OUTPUTS		
A	B	C	FBRK	A	B	C
0	0	0	0	OFF	OFF	OFF
1	0	0	0	1	OFF	0
0	1	0	0	0	1	OFF
1	1	0	0	OFF	1	0
0	0	1	0	OFF	0	1
1	0	1	0	1	0	OFF
0	1	1	0	0	OFF	1
1	1	1	0	OFF	OFF	OFF
X	X	X	1	0	0	0

* Undervoltage and Force Brake logic truth table entries are identical.

"X" = Don't Care

Absolute Maximum Ratings

Supply Voltage, SV+ or PV+ . . . . . -1V to +16V
Referred to SGND or PGND (Note 1)
Output Current, Continuous 3A
Output Current, Peak (Note 2) 5A
Substrate (PGND) Current 1A
Logic Input Current . . . . . -20mA to +20mA
(Clamped to SV+ and SGND)

Dissipation/Temperature Ratings

Power Dissipation (Note 3) 25W
Junction Temperature Range, Operating . . . . . +150°C
Storage Temperature Range . . . . . -55°C to +150°C

NOTES:

1. PV+ and SV+ are to be tied together, as are PGND and SGND.
2. Operating above the continuous current rating causes a decrease in operating life.
3. Derate power dissipation above case temperature of +75°C at 0.33 Watts/°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
SUPPLY (SV+) CURRENT					
No Drive	Outputs Off			10	mA
With Drive	Outputs On			15	mA
LOGIC INPUT CURRENT					
Sensor Inputs	SENA, SENB & SENC = 0V to 3V	-0.5		-1.5	mA
Brake Input	FBRK = 0.8V to 2.4V	50		150	µA
LOGIC INPUT THRESHOLDS					
Sensor Inputs	Logic "0" Input Voltage			1.8	V
Sensor Inputs	Logic "1" Input Voltage	3			V
Brake Input	Logic "0" Input Voltage			0.8	V
Brake Input	Logic "1" Input Voltage	2.4			V
AMPLIFIER INPUT (SPD)					
Bias Current				700	nA
Offset Voltage				3	mV
Input Range (Linear)		0		1	V
Input Impedance		1			MΩ
SYSTEM BANDWIDTH	(Note 1)		35		kHz
CURRENT LIMIT	Rsense = 0.20Ω		5		A
THERMAL LIMIT					
Threshold			155		°C
Hysteresis			40		°C
OUTPUT DRIVERS					
On Saturation (See Note 5)	Iout = 3A, Vpmos + Vnmos			2.2	V
On Saturation (See Note 5)	Iout = 0.6A, Vpmos + Vnmos			0.44	V
Off Leakage	PV+ > Vout > PGND or Isen			1	mA
Slew Rate	(See Note 2)		0.5		V/µS
FREEWHEEL DIODES					
Forward Drop	Iout = 1A			1.5	V

This page supersedes DB304 page 6-11

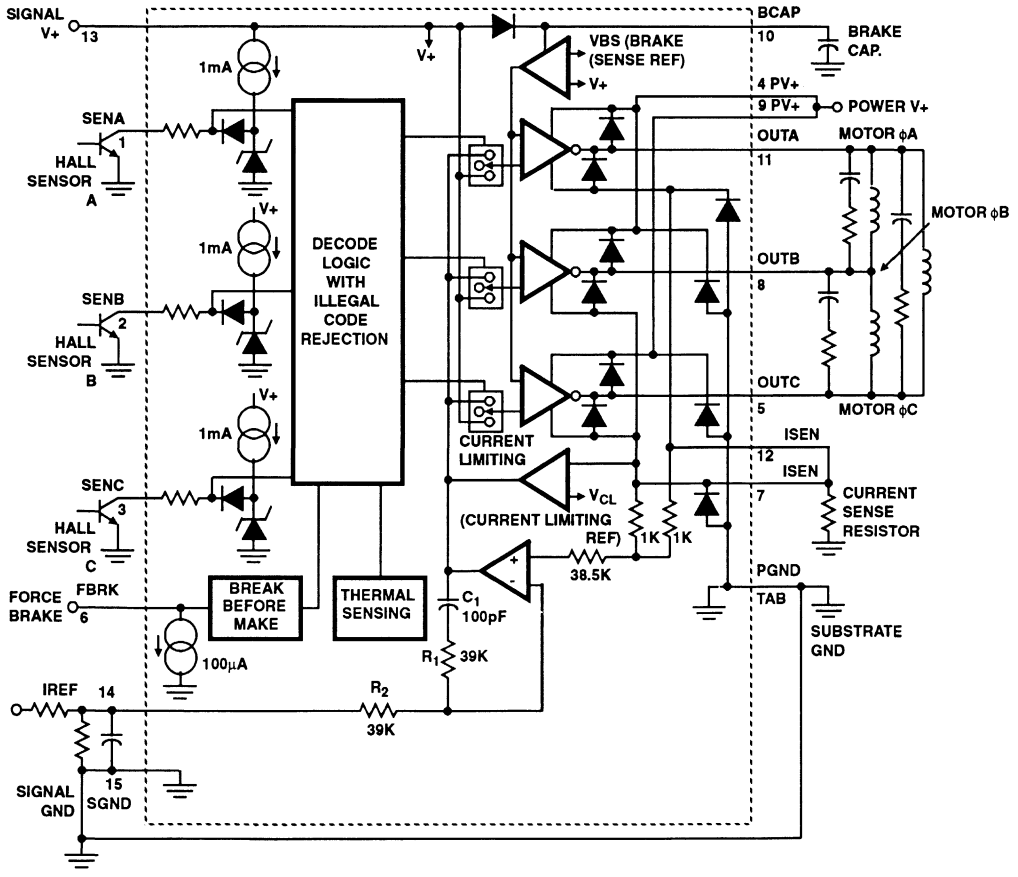
Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified (Continued)

CHARACTERISTIC	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INTERNAL BRAKE DRIVER					
Undervoltage Trip Point, PV+	(See Note 3)	2.7		3.3	V
Hysteresis	(See Note 4)	40		60	%
On Saturation	Each Nmos, Iout = 3A			0.4	V
BRAKE CAPACITOR (BCAP)					
Discharge Leakage	SV+ = PV+ = 3V to 12V, BCAP = 10V			5	µA

NOTES:

1. The system bandwidth is fixed by an internal RC network around the amplifier.
2. Internal limiting of turn on and turn off drive is used to limit output dv/dt.
3. The braking action starts at the given trip point with a falling supply voltage.
4. Hysteresis causes the brake to be removed at a higher trip point with a rising supply voltage.
5. This value includes the combined voltage drops of one upper plus one lower switch at the indicated current.

Functional Block Diagram



THREE-PHASE BRUSHLESS CONTROLLER

Harris Semiconductor

APPNOTE

No. AN9208 July 1992

Harris Intelligent Power

HIGH FREQUENCY POWER CONVERTERS

Authors: Rudy Severns, Springtime Enterprises
Hal Wittlinger, Harris Semiconductor

Introduction

Computers and telecom equipment are steadily becoming more complex, providing ever higher levels of performance. Simultaneously, the selling price for this equipment is being driven ever lower by market competition. Integral to all of this equipment is a power conversion system which converts the incoming unregulated power from the utility, or other source, to the multiple regulated voltages required by the equipment. In present designs the power subsystem constitutes a significant part of the equipment cost and volume.

The development of a unique power converter(s) for each new system is a substantial cost item in the equipment development. Frequently the equipment will have a variety of configurations with differing power requirements. To save development cost only a single design is often used to cover a range of loads. The result is that many users have to pay for capability not needed in their particular configuration.

One means to reduce power subsystem over capacity and cost is to use a distributed power system where the power processing functions are distributed within the system and more power processing capacity is added as required when more capability is installed. A typical distributed system will have a central power processor which converts the raw input power into a regulated DC bus. The central power processor is relatively simple but it does provide for line isolation and the safety requirements for the system. The central processor may be modular to allow for power scaling as the loads change. Each board or group of boards within the equipment has a small power processor which converts the DC bus to the voltages required by that particular section of the equipment. In general these board level converters are quite simple and efficient. Frequently no DC isolation is required at the board level which further simplifies the converters.

The use of multiple small power converters allows a custom system to be designed using high volume, low cost, standardized modules. In a complex system there can be substantial cost savings.

Board space is always at a premium and the localized power converters take up space. In general height is severely constrained and the power converter has a low profile geometry which tends to increase the board area required. In order to minimize the area required, the switching frequency (fs) of the converter is pushed as high as possible. The latest generation of systems [1] use converters with fs in the low MHz.

In addition to minimizing board area there are other requirements placed on these converters. [2] The components must be small enough for automated insertion and be low cost. All of this has to be achieved without seriously reducing conversion efficiency. Poor efficiency would increase the size and cost of the input converter and create thermal problems within the unit.

Overall these "simple" converters represent a significant design challenge.

Converter Circuits For MHz Switching

Many possible circuit topologies exist which could be used. They fall into three general categories: switchmode, resonant and quasi-resonant. At the power levels typical of board mounted converters (1 to 100W) single switch topologies are usually preferred for their lower cost. Examples of typical single switch, PWM converters are shown in Figure 1. A comparison of the switch, diode and capacitor voltages for these circuits is given in Table 1. In general circuits with the switch referenced to the ground node are preferred to simplify the switch drive circuits. The boost, Cuk and SEPIC circuits are non-isolated circuits with ground referenced switches. The flyback and forward converters provide isolation as well as multiple outputs with a single, ground referenced switch. The price paid for using an isolating transformer is higher cost and the increasing difficulty of designing a high performance transformer as the frequency is raised. The simpler non-isolated topologies are usually preferred in a distributed system unless there are compelling reasons to provide isolation.

TABLE 1. COMPONENT VOLTAGE STRESS FOR VARIOUS TOPOLOGIES

CIRCUIT	V_{SWITCH}	V_{DIODE}	$V_{COUPLING}$
Buck	V_I	V_I	N/A
Forward	$V_I/(1-D)$	$V_O/(1-D)$	N/A
Boost	V_O	V_O	N/A
Flyback	$V_I/(1-D)$	V_O/D	N/A
Buck-Boost	$V_I + V_O$	$V_I + V_O$	N/A
SEPIC	$V_I + V_O$	$V_I + V_O$	V_I
Cuk	$V_I + V_O$	$V_I + V_O$	V_I+V_O

NOTE: V_I = Input Voltage, V_O = Output Voltage, D = Duty Cycle

The boost, Cuk and SEPIC circuits each have different characteristics. The boost has a non-pulsating input current and a pulsating output current. It can only make voltages higher than the input bus. The Cuk converter has non-pulsating input and output currents and it can generate voltages either greater or less than the input voltage. The non-isolated Cuk converter inverts the sign of the input voltage. For the normal case of a positive DC bus, the Cuk converter will only produce negative voltages. The SEPIC converter is non-inverting and can generate voltages either above or below the input. The input current is non-pulsating but the output current is pulsating. Non-pulsating input and output currents are desirable to minimize EMI and reduce the need for additional filter elements.

The circuits in Figure 1 are considered "conventional" in that they have been widely used for many years. These topologies have first order input to output voltage transfer functions $M = V_O/V_I$, such as D, 1/(1-D) or D/(1-D). Recent work by Maksimovic [3, 4, 5] has shown that single switch quadratic and even higher order topologies exist. Three circuit examples are given in Figure 2. Quadratic circuits are particularly useful when large input to output voltage ratios are needed or a large variation in input voltage is present.

When implemented with discrete components the high frequency performance of switchmode circuits is limited by the parasitic inductance and capacitance normally present. This is due to the very fast voltage and current transitions required for efficient power conversion. One way to get

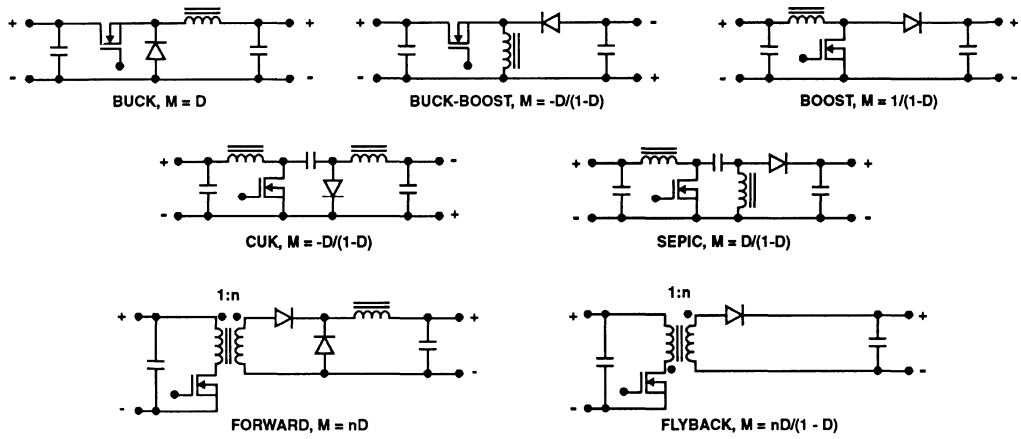


FIGURE 1. CONVERTER CIRCUITS, $M = V_O/V_I$

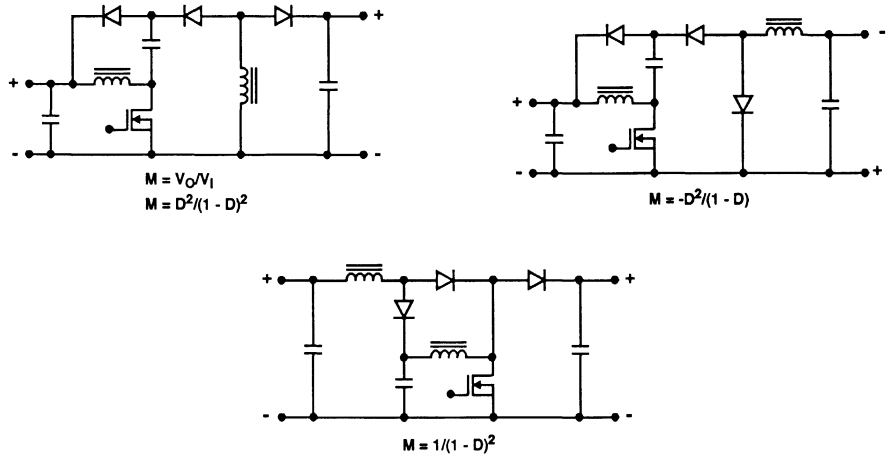


FIGURE 2. QUADRATIC CONVERTERS

around these problems is to modify the circuit such that it exploits the parasitic elements as part of normal operation. A boost version of a zero voltage switching quasi-resonant converter (ZVS-QRC) is shown in Figure 3. This is a typical example of this class of circuit. Many others exist [6, 7, 8, 9] and most switchmode topologies can be implemented as ZVS-QRC. This circuit operates quasi-resonant; i.e. during a portion of the switching cycle the waveforms are sinusoidal like a resonant converter and during other portions of the switching cycle the waveforms are essentially straight line segments like a non-resonant switchmode converter.

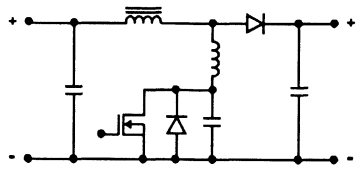
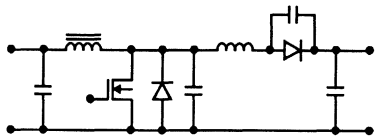


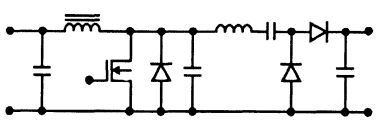
FIGURE 3. ZVS-QRC BOOST CONVERTER

The primary advantage of this topology is that the switch turns on and off while the voltage across the switch is zero. This translates to essentially zero switching loss and very low stress during switching transitions. The inherent junction capacitance of the switch is utilized as an active component as well as the series package inductance. This enables the switch to operate efficiently at very high frequencies (10MHz+). A price has to be paid for this performance. The converter can only be controlled by varying frequencies (fs). This is a relatively simple control scheme to implement but sometimes leads to EMI problems, particularly if the range of variation of fs is large. If fixed frequency operation is desired another switch must be added to the circuit. An additional disadvantage is that the switch voltage will be much higher than the input or output voltages. Peak switch voltages of 3 to 5 times the input voltage are typical. There are also restrictions on the acceptable load ranges and the switching frequency range can be large under some conditions.

Some improvement in performance can be obtained by operating the converter in a ZVS-multiresonant mode [10, 11]. Two examples are given in Figure 4. In this topology both the switch and the diode operate with low switching stress. This circuit does however, still have many of the disadvantages of the ZVS-QRC.



ZVS-MRC BOOST



CLASS E

FIGURE 4. MULTI-RESONANT CONVERTERS

Because of their disadvantages this family of converters is not usually employed until the operating frequency is so high that more conventional approaches cannot be used.

Many resonant converters can also be used for very high fs but in general they require more than a single switch and are not normally advantageous for low power levels (<100W).

Using Switchmode Circuits at MHz Frequencies

One of the primary motivations for developing resonant and quasi-resonant topologies has been to overcome the problems associated with switchmode converters when they are operated with high fs. While these approaches have been helpful, in general some price must be paid. This often takes the form of higher conduction losses, higher voltage stress, more numerous and larger components, loss of PWM control and limited load and input voltage ranges.

If the problems associated with high frequency operation can be overcome then switchmode circuits are advantageous. The limitations of switchmode converters for MHz operation stem primary from the difficulty of switching rapidly enough and the effect of parasitic components on the circuit behavior. An example of the parasitics present in a typical power stage is shown in Figure 5.

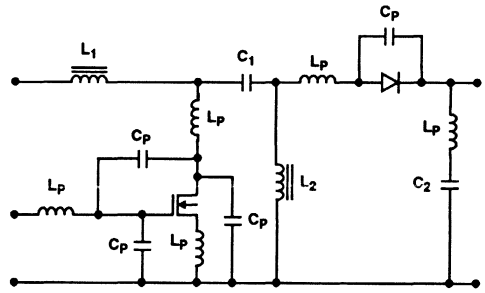


FIGURE 5. TYPICAL PARASITIC COMPONENTS

MOSFETs are inherently fast switching devices. If the input capacitance can be charged quickly enough they are capable of sub-nanosecond switching. However, in discrete or even hybrid circuits, the parasitic inductance in the gate and source connections limits the charge rate, increasing the switching transition time. The parasitic inductance and capacitance associated with the drain circuit causes voltage and current ringing which can over stress the switch and associated components, increase the switching loss and create VHF radiated and conducted EMI.

For power levels typically used in distributed power systems, a power IC manufactured with the Harris PASIC [12] (Power Applications Specific Integrated Circuit) process is an excellent way to minimize the parasitic elements that limit circuit performance and increase the level of integration. Other advantages of the PASIC technology is that the IC design can provide on-chip temperature monitoring and high speed, on-chip, current sensing. Moreover, on chip gate drivers help reduce and confine gate drive current and parasitic capacitance associated with external power transistors. Because the switch and its drive circuitry can be integrated

onto a very small area, nanosecond switching times are readily achieved. For volume production the IC has the advantage of much smaller size and lower cost than discrete equivalents.

Some external power components will still be needed, but they can be arranged to minimize parasitics. In the SEPIC converter shown in Figure 5, C_1 would be a chip ceramic capacitor and D_1 would be a surface mounted Schottky diode. Both of these components would be placed immediately adjacent to the IC. Efficient and economical 1MHz designs using this concept are presently in volume production.

It is possible to have floating or "high side" switches in the PASIC process for use with the buck topology shown in Figure 1. However, by using the SEPIC topology, the power DMOS transistor source may be returned to ground. This results in much simplified and efficient gate driving circuits. Moreover, a shorted or open power transistor is not detrimental to the load in the SEPIC topology. Because of the load coupling capacitor and the switch being returned to ground in the SEPIC topology, a shorted or open power transistor will not place the full high voltage input voltage on the load as in the buck topology. Besides the SEPIC topology, there is a host of topologies that may be implemented with a grounded source device, among them is the boost, forward, flyback, Cuk, and quadratic topologies.

The SEPIC Converter

The boost, Cuk, flyback and forward converters are well known to power supply designers and information on their design is widely available [13, 14 and 15]. The SEPIC topology has however, not been widely used. The following information is provided to familiarize designers with this circuit and its characteristics.

The name SEPIC is an acronym for Single-Ended Primary Inductance Converter. The circuit was first developed at AT&T Bell laboratories [16] in the mid 1970s. The intent of the developers was to create a new topology with properties not available in contemporary topologies. Of particular interest is the ability to buck or boost the input voltage without inverting voltage polarity.

A typical SEPIC circuit is shown in Figure 6A. This circuit has three dynamic energy storage elements, L_1, L_2 and C_1. The behavior of any switchmode circuit is strongly dependent on the continuity of the currents in the inductors and the voltages on the capacitors. A number of different operating modes are possible depending whether the inductor currents and capacitor voltages are continuous or discontinuous. As shown in Table 2, there are six possible inductor current operating modes. The -C entries are for conditions where one inductor current goes to zero before the other causing that inductor current to reverse direction. The inductor current is still continuous but the circuit behavior is different. The -D entries are for conditions where one inductor current goes negative and then a state exists where the two inductor currents are constant. The modes shown in Table 2 assume the voltage on C_1 is constant (small ripple). An additional set of modes is possible if the voltage on C_1 is discontinuous.

While all modes are possible, the usual operating mode is to have the voltage on C_1 continuous and either both L_1 and L_2 in continuous conduction or both L_1 and L_2 in discontinuous conduction. These two modes will be the only ones for which the circuit behavior will be derived in this applications note and will be referred to as the CCM and DCM modes, respectively. There is a brief discussion of four other modes which may be encountered.

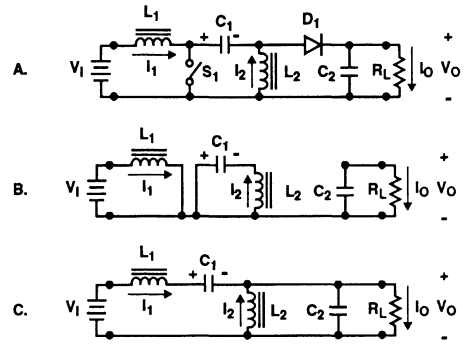


FIGURE 6. SEPIC CONVERTER

Table 2. SEPIC Operating Modes (C_1 and C_2 have small ripple)

INDUCTOR	CONDUCTION MODE					
L_1	D	C	C	-C	C	-D
L_2	D	C	-C	C	-D	C

CCM Circuit Operation

For this analysis it is assumed that both C_1 and C_2 are sufficiently large that the voltage ripple across them is small. By tracing the DC path from V_I through C_1, L_1, L_2 and back to V_I we see that $V_{C1} = V_I$. By inspection it can be seen that $V_{C2} = V_O$.

When S_1 is on, D_1 is off and when S_1 is off, D_1 is on. This means there are two circuit states during each switching cycle. The two states are shown in Figures 6B and 6C.

When S_1 is closed, L_1 is directly across V_I and I_1 is increasing. Energy is being stored in L_1. C_1 is connected across L_2 and I_2 is increasing. The energy in C_1 is being transferred to L_2. I_O is being maintained by C_2.

When S_1 is opened, the energy in L_1 is discharged into C_1 and C_2. The energy in L_2 is discharged into C_2. For CCM operation some energy remains in L_1 and L_2 (I_1 and $I_2 \neq 0$). At the end of the switching sequence S_1 is again closed and the cycle repeated.

To make the following discussion easier to follow, the details of the circuit analysis have been omitted. The equation derivations can be found in the appendix.

The ratio of the output voltage to the input voltage and the duty cycle are defined as:

$$M \equiv \frac{V_O}{V_I} \qquad \text{Equation 1}$$

$$D \equiv \frac{t_{ON}}{T} \qquad \text{Equation 2}$$

Where t_{ON} is the on time of S_1 and T = 1/fs, the switching period.

D as a function of M is:

$$D = \frac{M}{M+1} \qquad \text{Equation 3}$$

And M as a function of D is:

$$M = \frac{D}{1-D} \qquad \text{Equation 4}$$

A graph of Equation 4 is given in Figure 7 with comparisons to the buck, boost, Cuk and buck-boost converters. The large signal input-to-output voltage ratio for the SEPIC is identical to the Cuk and buck boost circuits except that there is no polarity inversion. V_O may be either less than or greater than V_I depending on D.

TABLE 3. SEPIC CCM VOLTAGES AND CURRENTS

M	V_O/V_I
D	$\frac{M}{M+1}$
M	$\frac{D}{1-D}$
$(I_1)_{RMS}$	MI_O
V_{L1}	V_O, M ≥ 1 and V_O/M, M ≤ 1
V_{S1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{S1})_{AVG}$	MI_O
$(I_{S1})_{RMS}$	$I_O\sqrt{M^2+M}$
V_{C1}	$V_O/M = V_I$
$(I_{C1})_{RMS}$	$I_O\sqrt{M}$
V_{L2}	V_O, M ≥ 1 and $V_O/M = V_I$, M ≤ 1
$(I_2)_{RMS}$	I_O
V_{D1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{D1})_{AVG}$	I_O
$(I_{D1})_{RMS}$	$I_O\sqrt{M+1}$
V_{C2}	V_O
$(I_{C2})_{RMS}$	$I_O\sqrt{M}$

Expressions for the voltages and currents in other circuit elements as a function of M, V_O and I_O are given in Table 3. Note that the expressions for the peak value for V_{L1} and V_{L2} depend on whether M > 1 or M < 1. The expressions in Table 3 assume that L_1 and L_2 are large with only small current ripple. For the case where the inductors are operating close the CCM-DCM boundary, the current waveforms will be triangular rather than rectangular and the RMS values will be approximately 15% higher.

The boundary between CCM and DCM modes will depend on several variables. For a given load resistance ($R_L=V_O/I_O$), fs and M, the values for the critical inductances of L_1 and L_2 are:

$$L_{1C} = \left[\frac{1}{2fs\,(M^2+M)}\right]R_L \qquad \text{Equation 5}$$

$$L_{2C} = \left[\frac{1}{2fs\,(M+1)}\right]R_L \qquad \text{Equation 6}$$

If the inductor values are higher than critical, then the converter will operate in CCM. If the values for the inductors are less than critical then the converter will operate in DCM.

The ratio of L_{2C} to L_{1C} is:

$$\frac{L_{2C}}{L_{1C}} = M \qquad \text{Equation 7}$$

A very important point here is that the currents in L_1 and L_2 go to zero simultaneously only if L_2/L_1 = M! If V_O is held constant and V_I is varied then the CCM-DCM transition will occur at some other point and will involve an intermediate mode.

In distributed power systems V_I is the DC bus and is normally relatively well regulated so the M varies only over a small range. In that type of an application, a smooth transition from both inductors in CCM to both in DCM will be possible. If L_2/L_1 does not equal M then the circuit behavior will be quite different.

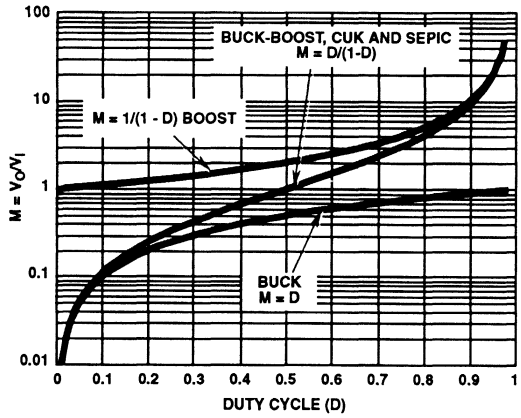


FIGURE 7. VOLTAGE TRANSFER AS FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

If I_2 reaches zero before I_1, D_1 will still be conducting because of the current in L_1. This means there will be a voltage across L_2 which reverses I_2. This leads to two additional operating modes. Current waveforms for the case where $I_1(T) > -I_2(T)$ are shown in Figure 8. This mode corresponds to the C, -C state in Table 2. Figure 9 shows the waveforms for the case where $I_1 = -I_2$ at $t < T$. In this mode, when $I_1 = -I_2$, D_1 drops out of conduction and a new operating state is introduced as shown. During this state (t_2 to T) the inductor currents are constant (ideally) because the voltage across C_1 cancels the input voltage. The conduction mode shown in Figure 8 is a continuous conduction mode but different from the continuous conduction mode where the current is unidirectional in both inductors. In the mode shown in Figure 9 the inductor currents are continuous but because of the period of time where di/dt = 0 (t_2 to T) the circuit will operate in a discontinuous mode. This mode corresponds to the C, -D mode in Table 2.

Both of these modes, C, -C and C, -D, have different characteristics from those mentioned in the previous discussion of continuous mode operation. The conditions where the current in L_1 reaches zero before the current in L_2 will be similar.

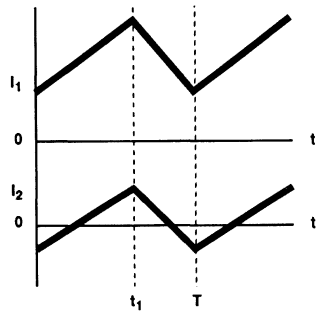


FIGURE 8. INDUCTOR CURRENTS FOR $I_1 > -I_2$ AT t = T

CCM Circuit Example

The following numerical example is provided to give a feeling for the component sizes and stresses in a typical application for the SEPIC converter.

Let:

$V_I = 35V$
$V_O = 12V$
$P_O = 50W$
fs = 1MHz

From this it can be seen that:

$I_O = 4.2A$
$R_L = 2.88\Omega$
M = 0.34

From Equations 5 and 6:

$L_{1C} = 3.2\mu H$
$L_{2C} = 1.1\mu H$

To operate weli within CCM and minimize the RMS currents let:

$L_1 = 5\mu H$
$L_2 = 1.7\mu H$

These inductors could be a single layer, wound on small powdered iron or NiZn ferrite cores. From the equations in Table 3:

$V_{S1} = 47V$
$(I_{S1})_{RMS} = 2.8A$ RMS

A MOSFET with $BV_{DSS} = 60V$ would be appropriate for S_1.

$V_{D1} = 47V$
$(I_{D1})_{AVG} = 4.2A$

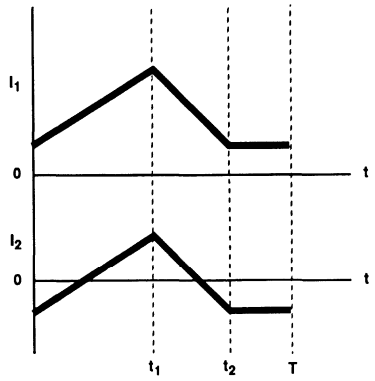
A 60V Schottky diode could be used for D_1.

$V_{C1} = 35V$
$(I_{C1})_{RMS} = 2.4A$ RMS

For C_1 a 50V, 0.47 to 1µF, multilayer, ceramic chip capacitor would be appropriate.

$V_{C2} = 12V$
$(I_{C2})_{RMS} = 2.4A$ RMS

For C_2 a 25V, 1µF, ceramic chip capacitor would be appropriate.



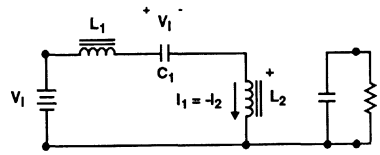


FIGURE 9. INDUCTOR CURRENTS AT $I_1 = I_2$ FOR t < T

DCM Circuit Operation

The following discussion assumes that $L_2/L_1 = M$ and that both inductors go into discontinuous conduction simultaneously.

Operation in the DCM mode adds an additional circuit state as shown in Figure 10. At t = 0, the point at which S_1 is turned on, I_1 and $I_2 = 0$. The current in both inductors will rise until S_1 turns off (Figure 10A). At that point the energy in the inductors is discharged into the output (Figure 10B). When the inductor currents reach zero, D_1 stops conducting and the final state is assumed (Figure 10C). No current flows in the inductors because the voltage on C_1 cancels V_I.

The expressions for D and M are:

$$D = \sqrt{2\tau_L\left[\frac{M^3}{M+1}\right]} \qquad \text{Equation 8}$$

Where:

$$\tau_L = \frac{fsL_1}{R_L} \qquad \text{Equation 9}$$

Equation 8 is only valid for D < 1. This sets an upper limit on τ_L of:

$$(\tau_L)_{MAX} = \frac{M+1}{2M^3} \qquad \text{Equation 10}$$

Values of τ_L greater than this limit mean that the converter is operating in CCM for the particular value of M.

Graphs of Equation 8 is given in Figures 11 and 12. These graphs illustrate the effect of varying load on the output voitage for M > 1 and M < 1.

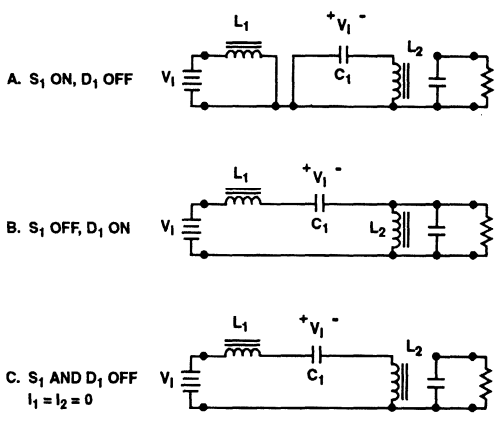


FIGURE 10. SEPIC DCM CIRCUIT STATES $L_2/L_1 = M$

Coupled Inductor Operation

Referring to Figure 6, when S_1 is closed, the voltage across both L_1 and L_2 is equal to V_I. From Figure 6B it can be seen that for the remainder of the switching cycle the voltage across L_1 and L_2 is equal to V_O. Because these two voltages are equal and in phase, L_1 and L_2 may be integrated into a single magnetic structure with only one magnetic path, this is referred to as a coupled inductor. A coupled inductor version of the SEPIC topology [14] is shown in Figure 13. This topology has several advantages. The leakage inductance of the coupled inductor can be arranged to effect zero current ripple on the input with finite value of L. Because the turns ratio between the windings is 1:1, there cannot be two different values for L_1 and L_2. This does not lead to multiple modes however. Because they are wound on a common core, both windings are either conducting or not depending on whether there is energy in the core or not. The circuit operates either CCM or DCM.

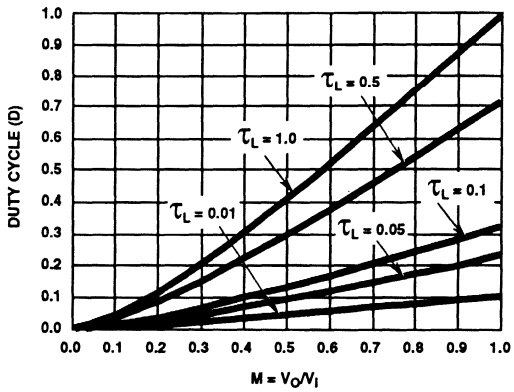


FIGURE 11. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 1

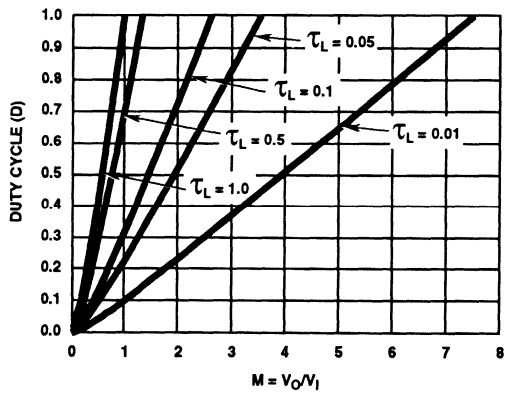


FIGURE 12. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 8

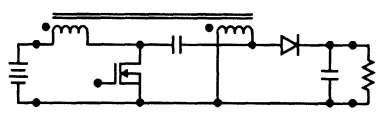


FIGURE 13. COUPLED INDUCTOR SEPIC

References

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Appendix

SEPIC Equation Derivations for CCM and DCM Operation CCM Operation

The following calculations are referenced to Figure 6.

For C_1 and C_2 large: $V_{C1} = V_I$ and $V_{C2} = V_O$

When S_1 is closed: $V_{L1} = V_{L2} = V_I$

When S_1 is open: $V_{L1} = V_{L2} = -V_O$

By conservation of flux in the inductors:

$$V_I t_{ON} = V_O (T - t_{ON}) \quad \text{(A1)}$$

For $D = t_{ON}/T$ and $M = V_O/V_I$ Equation A1 reduces to:

$$M = D/(1 - D) \quad \text{(A2)}$$

Equation A2 can be inverted:

$$D = M/(M + 1) \quad \text{(A3)}$$

Assuming that L_1 and L_2 are sufficiently large that the current ripple is small and substituting A3

$$I_O = (I_1 + I_2)(1 - D) = (I_1 + I_2)(1/(M + 1)) \quad \text{(A4)}$$

For Power In = Power Out: (A5)

$$V_I I_1 = V_O I_O,\ M = V_O/V_I = I_1/I_O$$

Combining Equations A4 and A5:

$$I_2 = I_O \quad \text{(A6)}$$

S_1 Voltage and Current

For S_1 open:

$$V_{S1} = V_{C1} + V_O = V_I + V_O \quad \text{(A7)}$$

Restating in terms of M and V_O:

$$V_{S1} = (1 + 1/M)V_O \quad \text{(A8)}$$

For S_1 closed:

$$(I_{S1})_{RMS} = (I_1 + I_2)\sqrt{D} \quad \text{(A9)}$$

Which reduces to:

$$(I_{S1})_{RMS} = I_O\sqrt{(M + M^2)} \quad \text{(A10)}$$

D1 Voltage and Current

By inspection:

$$(I_{D1})_{AVG} = I_O \quad \text{(A11)}$$

When S_1 is closed:

$$V_{D1} = V_I + V_O = (1 + 1/M)V_O \quad \text{(A12)}$$

Note the switch and diode have the same peak voltage.

Inductor Currents

$$(I_1)_{RMS} = I_1 = MI_O \quad \text{(A13)}$$

$$(I_2)_{RMS} = I_O \quad \text{(A14)}$$

This assumes small current ripple. If smaller inductors are used such that the inductor currents are nearly triangular (near the DCM-CCM boundary) the RMS current values will be approximately 15% higher.

Capacitor Currents

$$(I_{C1})_{RMS} = \sqrt{I_1^2(1-D)+I_2^2} \quad \text{(A15)}$$

Which reduces to: $(I_{C1})_{RMS} = I_O\sqrt{M}$ (A16)

$$(I_{C2})_{RMS} = \sqrt{I_O^2 D + (I_1 + I_2 - I_O)^2} \quad \text{(A17)}$$

Which reduces to: $(I_{C2})_{RMS} = I_O\sqrt{M}$ (A18)

Values for the Critical Inductances of L_1 and L_2

For a given current, the critical inductance is the value for the inductor that allows the current to just reach zero at the end of the switching cycle. This is a special case of CCM.

L_1 Critical

The input current will be triangular. I_{1P} = peak value of the current:

$I_{1P} = 2I_{1AVG} = 2MI_O$ (A19)

$I_{1P} = V_I t_{ON}/L1$ (A20)

$t_{ON} = DT$ (A21)

$fs = 1/T$ (A22)

Combining Equations A19 - A22:

$L_{1C} = [1/2fsM(M + 1)]R_L$ (A23)

A similar calculation for L_2 yields:

$L_{2C} = R_L/(2fs(M + 1))$ (A24)

DCM Analysis

For this analysis it will be assumed that:

$L_{2C}/L_{1C} = M$ (A25)

This means I_1 and I_2 go to zero simultaneously. The circuit states shown in Figure 10 will be used for this analysis.

$t_1 = t_{ON}$ = on time of S_1

t_2 = the current fall time in the inductors

From conservation of flux in L_1 and L_2:

$V_I t_1 = V_O t_2$ (A26)

From conservation of charge in C_1 (A27)

$I_{1AVG}t_2 = I_{2AVG}t_1$

From conservation of power: (A28)

$V_I I_{1AVG} = V_O I_O$

Derivation of Expressions for M and D

$I_{1P} = V_I t_1/L_1$ (A29)

$$I_{1AVG} = I_{1P}\left[\frac{t_1 + t_2}{2T}\right] \quad \text{(A30)}$$

Combining Equation A27 through A30:

$$D = \sqrt{\left[\frac{2fsL_1}{R_L}\right]\left[\frac{M^3}{M+1}\right]} \quad \text{(A31)}$$

INTELLIGENT POWER ICs 12

PACKAGING AND ORDERING INFORMATION

Part Number - Package Outline Designator

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
CA723E	14 Lead Dual-In-Line Plastic Package	E14.3
CA723T	10 Lead TO-5 Style Package	T10.A
CA723CE	14 Lead Dual-In-Line Plastic Package	E14.3
CA723CT	10 Lead TO-5 Style Package	T10.A
CA1523E	14 Lead Dual-In-Line Plastic Package	E14.3
CA1524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA1524F	16 Lead Frit Seal Ceramic Package	F16.3
CA2524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA2524F	16 Lead Frit Seal Ceramic Package	F16.3
CA3059	14 Lead Dual-In-Line Plastic Package	E14.3
CA3079	14 Lead Dual-In-Line Plastic Package	E14.3
CA3059H	Dice	N.A.
CA3079H	Dice	N.A.
CA3085, A, B	8 Lead TO-5 Style Package (TO-99)	T8.A
CA3085S, AS, BS	8 Lead TO-5 Style with Dual-In-Line Formed Leads	T8.B
CA3085E, AE, BE	8 Lead Dual-In-Line Plastic Package	E8.3
CA3085H	Dice	N.A.
CA3165E	8 Lead Dual-In-Line Plastic Package	E8.3
CA3165EI	14 Lead Dual-In-Line Plastic Package	E14.3
CA3169	5 Lead Plastic Single-In-Line Package	Z5.067
CA3228E	24 Lead Dual-In-Line Plastic Package	E24.6
CA3237E	9 Lead Single-In-Line Plastic Package	Z9.1
CA3242E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3262E, AE	16 Lead Dual-In-Line Plastic Package	E16.3
CA3262AQ	28 Lead Plastic Chip Carrier Package	N28.45
CA3272	28 Lead Plastic Chip Carrier Package	N28.45
CA3273	3 Lead Plastic Single-In-Line Package	Z3.1A
CA3274E	8 Lead Dual-In-Line Plastic Package	E8.3
CA3275E	14 Lead Dual-In-Line Plastic Package	E14.3
CA3277E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3282AS1	15 Lead Plastic Single-In-Line Package (Staggered Vertical Lead Form)	Z15.05A
CA3282AS2	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
CA3292Q	28 Lead Plastic Chip Carrier Package	N28.45
CA3524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3524F	16 Lead Frit Seal Ceramic Package	F16.3
CA3524H	Dice	N.A.

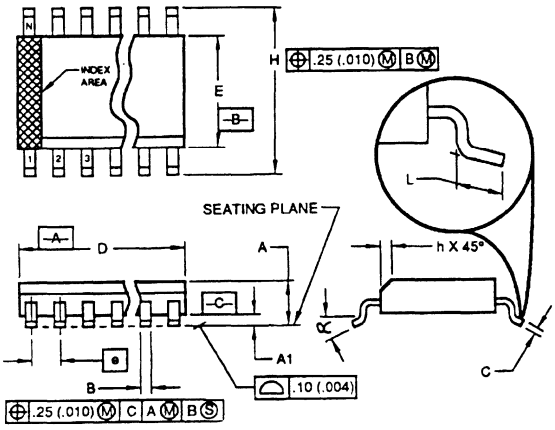
Part Number - Package Outline Designator (Continued)

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
HIP0080AM	28 Lead Plastic Chip Carrier Package	N28.45
HIP0081AS1	15 Lead Plastic Single-In-Line Package (Staggered Vertical Lead Form)	Z15.05A
HIP0081AS2	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
HIP1030AS	5 Lead Plastic Single-In-Line Package	Z5.067
HIP2500IP	14 Lead Dual-In-Line Plastic Package	E14.3
HIP4010MP	16 Lead Dual-In-Line Plastic Package	E16.3
HIP4011IS	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
HIP4080IP	20 Lead Dual-In-Line Plastic Package	E20.3
HIP4080IB	20 Lead Small Outline Plastic Package	M20.3
HIP5060DY	Dice	N.A.
HIP5060DW	Wafer	N.A.
HIP5061DS	7 Lead Plastic Single-In-Line Package Staggered Surface Mount "Gullwing" Lead Form	Z7.05A
HIP5062DY	Dice	N.A.
HIP5062DW	Wafer	N.A.
HIP5063DY	Dice	N.A.
HIP5063DW	Wafer	N.A.
HIP5500IP	20 Lead Dual-In-Line Plastic Package	E20.3
HIP5500IB	24 Lead Small Outline Plastic Package	M24.3
HIP9020AP	14 Lead Dual-In-Line Plastic Package	E14.3
HIP9020AB	20 Lead Small Outline Plastic Package	M20.3
HV3-2405E-5, -9	8 Lead Dual-In-Line Plastic Package	E8.3
HV400CB, IB	8 Lead Small Outline Plastic Package	M8.15
HV400CP, IP	8 Lead Dual-In-Line Plastic Package	E8.3
HV400Y	Dice	N.A.
ICL7644CPD, 45CPD, 46CPD, 47CPD	14 Lead Dual-In-Line Plastic Package	E14.3
ICL7644CBD, 45CBD, 46CBD, 47CBD	14 Lead Small Outline Plastic Package	M14.15
ICL7644IPD, 45IPD, 46IPD, 47IPD	14 Lead Dual-In-Line Plastic Package	E14.3
ICL7644IBD, 45IBD, 46IBD, 47IBD	14 Lead Small Outline Plastic Package	M14.15
ICL7660CTV, MTV	8 Lead TO-5 Style Package (TO-99)	T8.A
ICL7660CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7660CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7660SCBA, IBA	8 Lead Small Outline Plastic Package	M8.15
ICL7660SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7660SCTV, ITV, MTV	8 Lead TO-5 Style Package (TO-99)	T8.A

Part Number - Package Outline Designator (Continued)

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
ICL7662CTV, MTV	8 Lead TO-5 Style Package (TO-99)	T8.A
ICL7662CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7662MCBD	14 Lead Small Outline Plastic Package	M14.15
ICL7663SCBA, IBA	8 Lead Small Outline Plastic Package	M8.15
ICL7663SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7663SCJA, IJA	8 Lead Frit Seal Ceramic Package	F8.3
ICL7663SACPA, AIPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7663SACJA, AIJA	8 Lead Frit Seal Ceramic Package	F8.3
ICL7665SCBA, IBA	8 Lead Small Outline Plastic Package	M8.15
ICL7665SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7665SCJA, IJA	8 Lead Frit Seal Ceramic Package	F8.3
ICL7665SACPA, AIPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7665SACJA, AIJA	8 Lead Frit Seal Ceramic Package	F8.3
ICL7667CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7667CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7667CJA, MJA	8 Lead Frit Seal Ceramic Package	F8.3
ICL7667CTV, MTV	8 Lead TO-5 Style Package (TO-99)	T8.A
ICL7673CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7673CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7673ITV	8 Lead TO-5 Style Package (TO-99)	T8.A
ICL8211CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL8211CBA	8 Lead Small Outline Plastic Package	M8.15
ICL8211CTY, MTY	8 Lead TO-5 Style Package (TO-99)	T8.A
ICL8212CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL8212CBA	8 Lead Small Outline Plastic Package	M8.15
ICL8212CTY, MTY	8 Lead TO-5 Style Package (TO-99)	T8.A
SP600	22 Lead Dual-In-Line Plastic Package	E22.4
SP601	22 Lead Dual-In-Line Plastic Package	E22.4
SP710AS	3 Lead Plastic Single-In-Line Package	Z3.1B
SP720AP	16 Lead Dual-In-Line Plastic Package	E16.3
SP720AB	16 Lead Small Outline Plastic Package	M16.15

Small Outline (SO) Plastic Packages



M8.15 (JEDEC MS-012-AA)
8 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

M14.15 (JEDEC MS-012-AB)
14 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

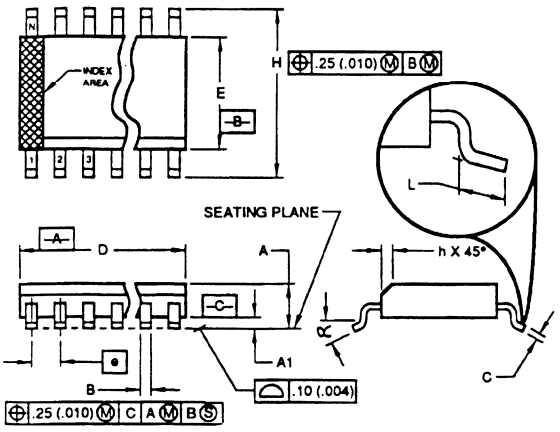
M16.15 (JEDEC MS-012-AC)
16 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

NOTES:

1. Refer to applicable symbol List.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline (SO) Plastic Packages (Continued)



M20.3 (JEDEC MS-013-AC)
20 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

NOTES:

1. Refer to applicable symbol List.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD)
24 LEAD SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Dual-In-Line Plastic Packages

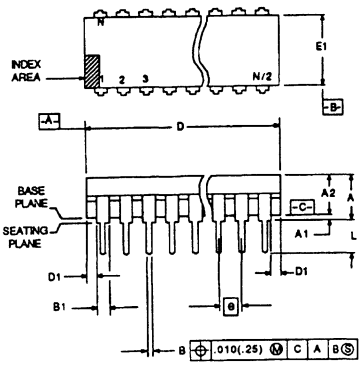


FIGURE 1

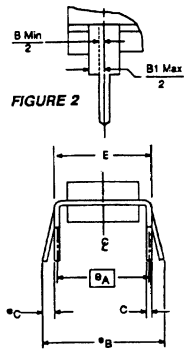


FIGURE 2

E8.3 (JEDEC MS-001-AB)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A_1	0.015	-	0.39	-	4
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.348	0.430	8.84	10.92	5
D_1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E_1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	8		8		8

E14.3 (JEDEC MS-001-AC)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A_1	0.015	-	0.39	-	4
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.725	0.795	18.42	20.19	5
D1	0.005	-	0.13		-
E	0.300	0.325	7.62	8.25	6
E_1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	14		14		8

E16.3 (JEDEC MS-001-AA)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A_1	0.015	-	0.39	-	4
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.745	0.840	18.93	21.33	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E_1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	16		16		8

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A_1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E_1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

Dual-In-Line Plastic Packages (Continued)

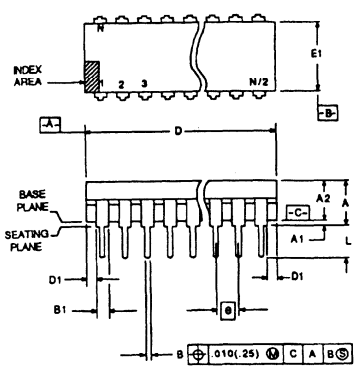


FIGURE 1

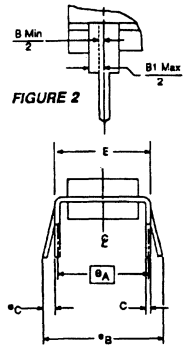


FIGURE 2

E20.3 (JEDEC MS-001-AE)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A_1	0.015	-	0.39	-	4
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.0450	0.070	1.55	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.925	1.060	23.5	26.9	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E_1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	20		20		8

E22.4 (JEDEC MS-010-AA)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A_1	0.015	-	0.39	-	4
A_2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.050	1.120	26.67	28.44	5
D_1	0.005	-	0.13	-	-
E	0.390	0.425	9.91	10.79	6
E_1	0.330	0.380	8.39	9.65	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		8

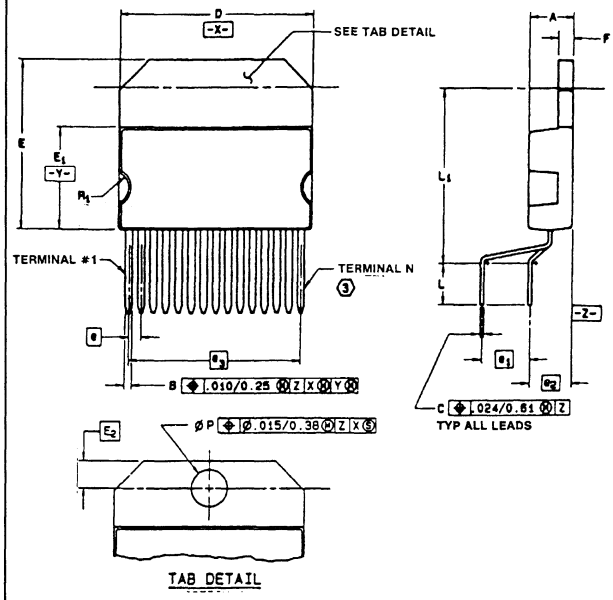
E24.6 (JEDEC MS-011-AA)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A_1	0.015	-	0.39	-	4
A_2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.77	1.77	9
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	-
E	0.600	0.625	15.24	15.87	6
E_1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		8

NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A_1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

Single-In-Line Plastic Packages (SIP)



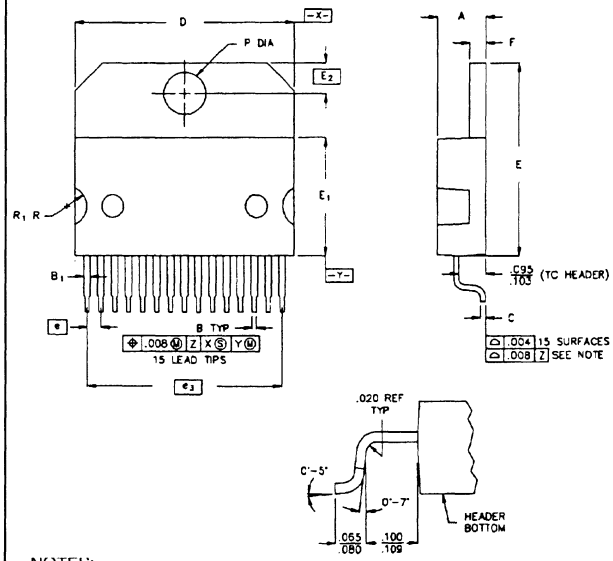
Z15.05A (JEDEC MO-048 AB)

15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
STAGGERED VERTICAL LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E_1	0.416	0.426	10.57	10.82
E_2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e_1	0.200 BSC		5.08 BSC	
e_2	0.169 BSC		4.29 BSC	
e_3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
P	0.148	0.152	3.76	3.86
R_1	0.065	0.080	1.65	2.03

NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: Inch.



Z15.05B

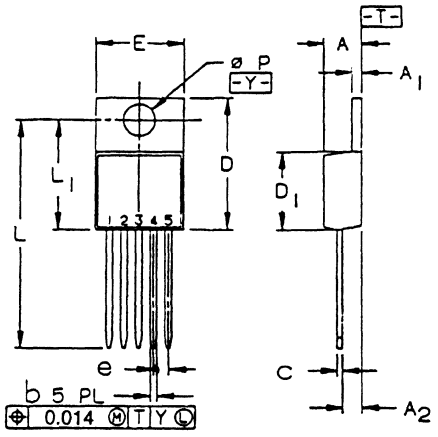
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
SURFACE MOUNT 'GULLWING' LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.020	0.024	0.31	0.61
B_1	0.024	0.031	0.61	0.79
C	0.018	0.024	0.46	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E_1	0.416	0.426	10.57	10.82
E_2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e_3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
N	15		15	
P	0.148	0.152	3.76	3.86
R_1	0.065	0.080	1.65	2.03

NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M - 1982.
3. N is the number of terminals.
4. Lead surfaces within 0.004 inch of each other. No lead can be more than 0.004 inch from header plane.
5. Controlling dimension: Inch

Single-In-Line Plastic Packages (SIP) (Continued)



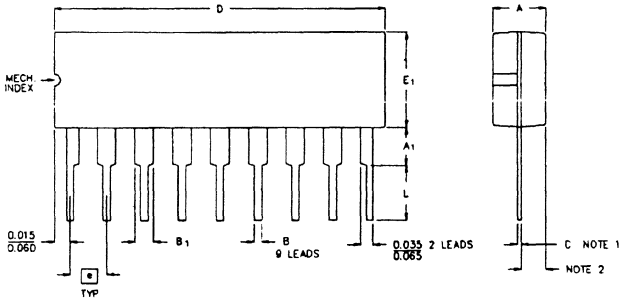
Z5.067 (JEDEC TS-001)

5 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.190	4.19	4.82
A_1	0.035	0.055	0.89	1.39
A_2	0.085	0.115	2.16	2.92
b	0.020	0.040	0.51	1.01
c	0.012	0.025	0.31	0.63
D	0.570	0.625	14.48	15.87
D_1	0.330	0.370	8.39	9.39
e	0.067 BSC		1.70 BSC	
E	0.390	0.415	9.91	10.54
L	0.945	1.045	24.00	26.54
L_1	0.465	0.539	11.81	13.69
P	0.139	0.156	3.53	3.96

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
3. Controlling dimension: inch.



Z9.1

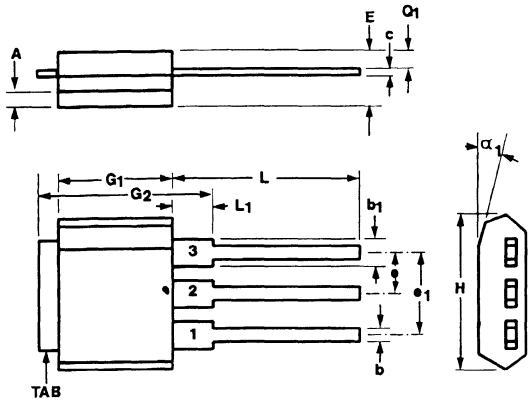
9 LEAD SINGLE-IN-LINE PLASTIC (SIP)

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.140	-	3.56
A_1	0.090	0.120	2.29	3.05
B	0.014	0.020	0.36	0.51
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.845	0.885	21.47	22.48
E_1	0.240	0.260	6.10	6.61
e	0.100 BSC		2.54 BSC	
L	0.125	0.150	3.18	3.81
N	9		9	

NOTES:

1. A maximum of 0.013 inch on the lead thickness is to be maintained after solder coating on the narrow portion of the lead.
2. Lead within 0.010 inch radius of true position (TP) with maximum material condition.
3. Controlling dimension: Inch

Single-In-Line Plastic Packages (SIP) (Continued)

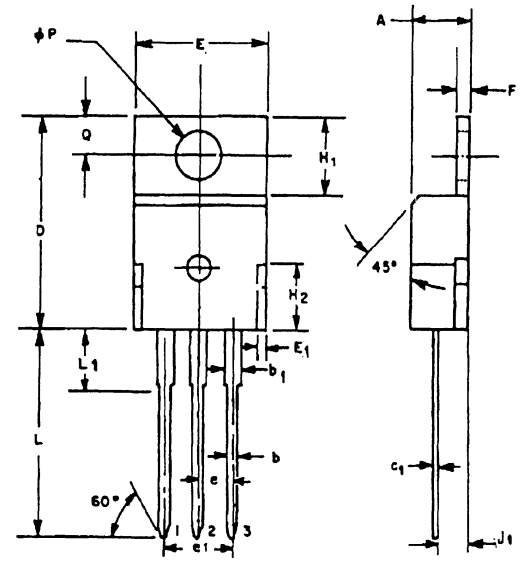


Z3.1A (JEDEC TO-202 MODIFIED)
3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.050	-	1.270	1
b	0.023	0.029	0.584	0.736	-
b_1	0.045	0.055	1.143	1.397	1
c	0.018	0.026	0.457	0.660	-
E	0.130	0.150	3.302	3.810	-
e	0.095	0.105	2.413	2.667	-
e_1	0.190	0.210	4.826	5.334	-
G_1	0.220	0.260	5.588	6.624	-
G_2	0.415	0.425	10.54	10.80	-
H	0.330	0.380	8.362	9.652	-
L	0.390	0.450	9.906	11.43	-
L_1	-	0.110	-	2.794	1, 2
Q_1	0.039	0.050	0.990	1.270	-
α_1	-	50°	-	50°	1

NOTES:

1. Package contour optional within dimensions specified.
2. Lead dimensions uncon trolled in this zone.



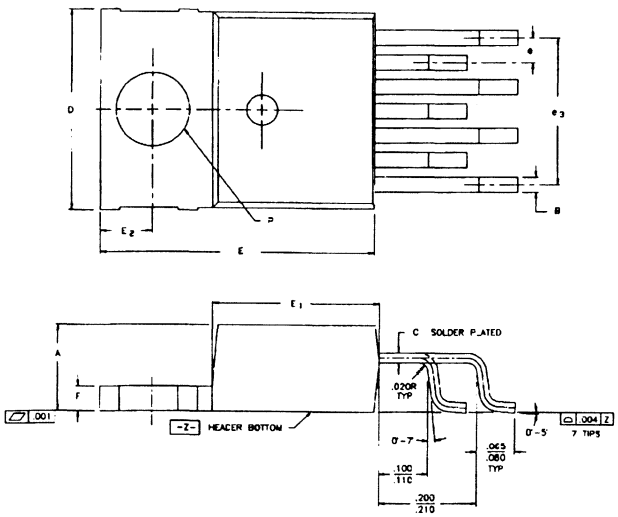
Z3.1B (JEDEC TO-220AB)
3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.190	3.56	4.82	-
b	0.015	0.040	0.38	1 02	-
b_1	0.045	0.070	1.14	1.77	-
c_1	0.014	0.022	0.36	0.56	-
D	0.560	0.625	14.23	15.87	-
E	0.380	0.420	9.66	10.66	-
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
E_1	-	0.030	-	0.76	-
F	0.020	0.055	0.51	1.39	-
H_1	0.230	0.270	5.85	6.85	-
H_2	-	0.165	-	4.19	-
J_1	0.080	0.115	2.04	2.92	-
L	0.500	0.562	12.70	14.27	-
L_1	-	0.250	-	6.35	-
ϕP	0.139	0.153	3.53	3.89	-
Q	0.100	0.135	2.54	3.43	-

NOTES:

1. These dimensions are within allowable dimensions of revision J of JEDEC TO-220AB outline dated 3-24-87.
2. Position of lead to be measured 0.250 - 0.255 (6.350 - 6.477mm) from case.

Single-In-Line Plastic Packages (SIP) (Continued)



Z7.05A

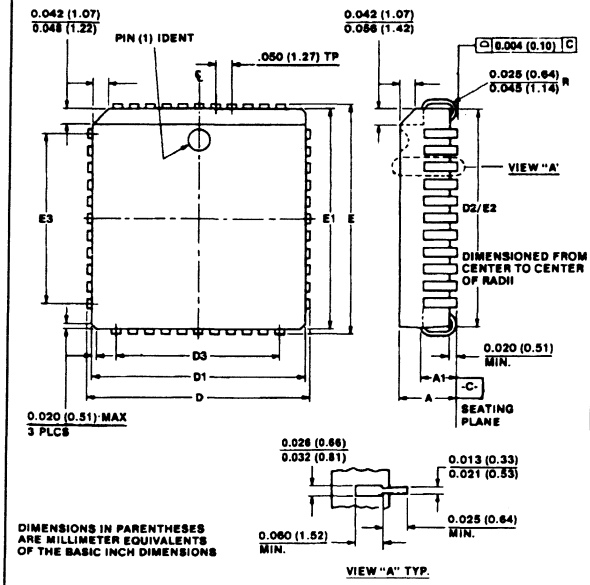
7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE STAGGERED SURFACE MOUNT "GULLWING" LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.190	4.06	4.83
B	0.023	0.037	0.58	0.94
C	0.015	0.022	0.38	0.56
D	0.385	0.415	9.78	10.54
E	0.560	0.590	14.22	14.99
E_1	0.326	0.332	8.28	8.43
E_2	0.103	0.113	2.62	2.87
e	0.045	0.055	1.14	1.40
e_3	0.295	0.305	7.49	7.75
F	0.045	0.055	1.14	1.40
N	7		7	
P	0.145	0.156	3.68	3.98

NOTES:

1. Refer to applicable symbol list, JEDEC Publication No. 95.
2. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
3. N is the number of leads.
4. Controlling dimension: Inch.

Plastic Leaded Chip Carrier Packages



N28.45 (JEDEC MO-047AB)

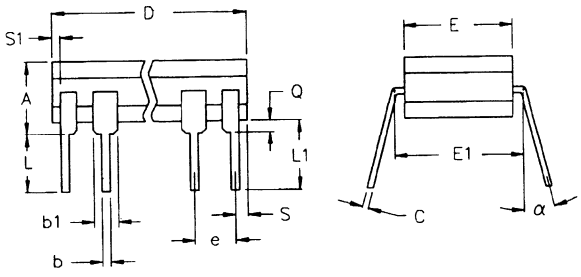
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A_1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D_1	0.450	0.456	11.430	11.582	2
D_2	0.390	0.430	9.91	10.92	1
D_3	0.300 REF		7.62 BSC		-
E	0.485	0.495	12.32	12.57	-
E_1	0.450	0.456	11.430	11.582	2
E_2	0.390	0.430	9.91	10.92	1
E_3	0.300 REF		7.62 BSC		-
N	28		28		3

NOTES:

1. To be determined at seating plane.
2. Dimensions D_1 and E_1 do not include mold protrusions. Allowable mold protrusion is 0.254mm/0.010 inch.
3. "N" is the number of terminal positions.
4. Controlling dimenstion: inch.

Dual-In-Line Frit-Seal Ceramic (Cerdip) Packages



F8.3

8 LEAD FRIT SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.023	0.36	0.58	8
b_1	0.045	0.065	1.14	1.65	2, 8
C	0.008	0.015	0.20	0.38	8
D	-	0.410	-	10.41	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	-
L_1	0.150	-	3.81	-	-
N	8		8		9
Q	0.015	0.060	0.38	1.52	3
S	-	0.065	-	1.65	6
S_1	0.005	-	0.13	-	6
α	0°	15°	0°	15°	-

NOTES:

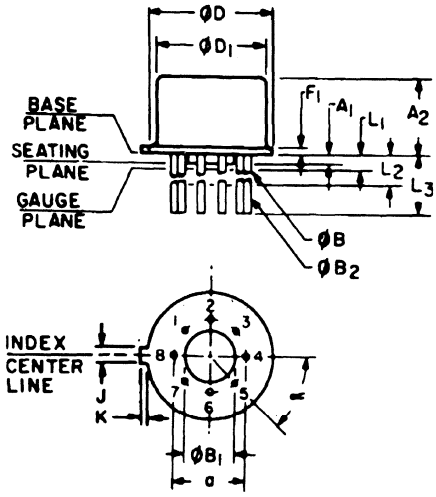
1. Index area; a notch or a lead one identification mark shall be located adjacent to lead one. The manufacturer's identification shall not be used as a lead one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 inch (0.58mm) for corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54mm) between centerlines. Each lead centerline shall be located within ±0.010 inch (0.25mm) of its exact longitudinal position relative to leads 1 and N.
6. Applies to all four corners.
7. E_1 shall be measured at the center of the lead bends.
8. All leads increase maximum limit by 0.003 inch (0.08mm) measured at the center of the flat, when lead finish A is applied.
9. N is the maximum quantity of lead positions.

F16.3

16 LEAD FRIT SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.023	0.36	0.58	8
b_1	0.045	0.065	1.14	1.65	2, 8
C	0.008	0.015	0.20	0.38	8
D	-	0.840	-	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	-
L_1	0.150	-	3.81	-	-
N	16		16		9
Q	0.015	0.060	0.38	1.52	3
S	-	0.080	-	2.03	6
S_1	0.005	-	0.13	-	6
α	0°	15°	0°	15°	-

TO-5 Style Packages



T8.A
8 LEAD TO-5 STYLE PACKAGE (TO-99)

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.200 TP		5.88 TP		1
A_1	0.010	0.050	0.26	1.27	-
A_2	0.165	0.185	4.20	4.69	-
$ø_B$	0.016	0.019	0.407	0.482	2
$øB_1$	0.110	0.160	2.79	4.06	-
$øB_2$	0.016	0.021	0.407	0.482	2
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	-	0.040	-	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.027	0.045	0.69	1.14	3
L_1	0.000	0.050	0.000	1.27	2
L_2	0.250	0.500	6.4	12.7	2
L_3	0.500	0.562	12.7	14.27	2
α	45° TP		45° TP		-
N	8		8		5
N_1	3		3		4

T10.A (JEDEC MO-006-AF)
10 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.230 TP		5.84 TP		1
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	2
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	2
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	-	0.040	-	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	3
L_1	0.000	0.050	0.000	1.27	2
L_2	0.250	0.500	6.4	12.7	2
L_3	0.500	0.562	12.7	14.27	2
α	36°TP		36° TP		-
N	10		10		5
N_1	1		1		4

T12.A (JEDEC MO-006-AG)
12 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.230 TP		5.84 TP		1
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	2
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	2
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	3
L_1	0.000	0.050	0.000	1.27	2
L_2	0.250	0.500	6.4	12.7	2
L_3	0.500	0.562	12.7	14.27	2
α	30°TP		30° TP		-
N	12		12		5
N_1	1		1		4

NOTES:

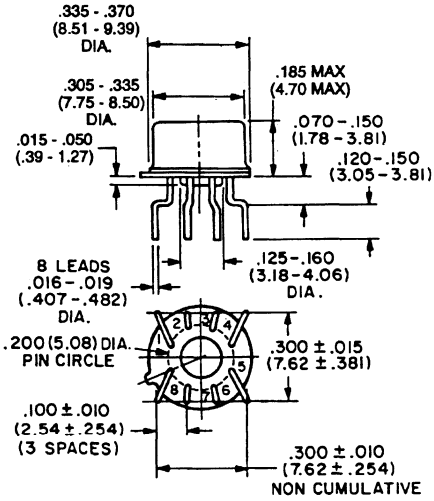
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. Leads at gauge plane within 0.007 inch (0.178mm) radius of True Position (TP) at maximum material condition.
2. ØB applies between L1 and L2. ØB2 applies between L2 and 0.500 inch (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.500 inch (12.70mm).
3. Measure from maximum ØD.
4. N1 is the quantity of allowable missing leads.
5. N is the maximum quantity of lead positions.

TO-5 Style Packages (Continued)

T8.B

8 LEAD TO-5 STYLE WITH DUAL-IN-LINE FORMED LEADS (DILCAN)



All Dimensions Given in: Inches / (Millimeters)